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(54) Title: METHOD OF CONVERTING A SERIES OF M-BIT INFORMATION WORDS TO A MODULATED SIGNAL, METHOD OF PRODUCING A RECORD CARRIER, CODING DEVICE, DECODING DEVICE, RECORDING DEVICE, READING DEVICE, SIGNAL, AS WELL AS A RECORD CARRIER

(57) Abstract

The Patent Applications relates to a method of converting a series of m-bit information words (1) to a modulated signal (7). For each information word from the series an n-bit code word (4) is delivered. The delivered code words (4) are converted to the modulated signal (7). The code words (4) are distributed over at least one group (G11, G12) of a first type and at least one group (G2) of a second type. For the delivery of each of the code words belonging to the group (G11, G12) of the first type the associated group establishes a coding state (S1, S4) of the first type. When each of the code words (4) belonging to the group (G2) of the second type is delivered, a coding state (S2, S3) of the second type is established which is determined by an information word belonging to the delivered code word. When one of the code words (4) is assigned to the received information word (1), this code word is selected from a set (V1, V2, V3, V4) of code words which depends on the coding states (S1, S2, S3, S4). The sets of code words (V2, V3) belonging to the coding states (S1, S2) of the second type are disjunct. In this coding method the number of unique bit combinations that may be established by the code words in the series are enlarged. The modulated signal (7) thus obtained may be reconverted to information words (4) by first converting the modulated signal (7) to a series of code words (4) and then assigning an information word (1) to each of the code words from the series in dependence on the code word to be converted and also in dependence on the logical values of the bit string bits which are situated at predetermined positions relative to the code word. Furthermore, a recording device and a reading device are disclosed.

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Method of converting a series of m-bit information words to a modulated signal, method of producing a record carrier, coding device, decoding device, recording device, reading device, signal, as well as a record carrier.

The invention relates to a method of converting a series of m-bit information words to a modulated signal, with m being an integer, in which method an n-bit code word is delivered for each received information word, with n being an integer exceeding m, and the delivered code words are converted to the modulated signal, and in which the series of information words is converted to a series of code words according to rules of conversion, so that the corresponding modulated signal satisfies a predetermined criterion.

The invention further relates to a method of producing a record carrier on which a signal is recorded obtained according to said method.

The invention further relates to a coding device for performing the method as claimed, this device comprising an m-to-n bit converter for converting the m-bit information words to n-bit code words, and means for converting the n-bit code words to a modulated signal.

The invention further relates to a recording device in which a coding device of this type is used.

The invention further relates to a signal.

The invention further relates to a record carrier on which the signal is recorded.

The invention further relates to a decoding device for converting the signal to a series of m-bit information words, this device comprising converting means for converting the signal to a bit string of bits having a first or second logical value, this bit string containing n-bit code words which correspond to the information signal portions, and this device comprising converting means for converting the series of code words to the series of information words, while a codeword-dependent information word is assigned to each of the code words to be converted.

Finally, the invention relates to a reading device in which a decoding device of this type is used.

Such methods, such devices, such a record carrier and such a signal are published by K.A. Schouhamer Immink in the book entitled "Coding Techniques for Digital

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Recorders" (ISBN 0-13-140047-9). In said title, for example, the so-called EFM modulation system is described which is used for recording information on so-called Compact Discs. The EFM-modulated signal is obtained by converting a series of 8-bit information words to a series of 14-bit code words, three merging bits being inserted into the code words. The code words are selected such that the minimum number of "0" bits situated between the "1" bits is d (2) and the maximum number is k (10). This constraint is also referenced dk-constraint. The series of code words is converted, *via* a modulo-2 integration operation, to a corresponding signal formed by bit cells having a high or low signal value, a "1"-bit being represented in the modulated signal by a change from the high to the low signal value or *vice versa*. A "0"-bit is represented by the lack of a change of signal value at a transition between two bit cells. The merging bits are selected such that even in the regions of transition between two code words the dk-constraint is satisfied and that in the corresponding signal the so-called running digital sum value remains substantially constant. The running digital sum value at a specific instant is understood to mean the difference between the number of bit cells having the high signal value and the number of bit cells having the low signal value, calculated over the modulated signal portion situated before this instant. A substantially constant running digital sum value means that the frequency spectrum of the signal does not comprise frequency components in the low frequency area. Such a signal is also referenced a DC-free signal. The lack of low-frequency components in the signal is highly advantageous when the signal is read from a record carrier on which the signal is recorded in the track, because then continuous tracking control unaffected by the recorded signal is possible. Information recording has a constant need for enhancing the information density on the record carrier.

A possible solution to this is a reduction of the number of bit cells per information word in the modulated signal. However, the problem occurring then is that as a result of the reduction of this number of bit cells per information word the number of unique bit combinations which may represent the information words will decrease, due to which less strict constraints can be imposed on the modulated signal, for example, constraints as regards low-frequency contents of the modulated signal.

It is an object of the invention to provide means for reducing the number of bit cells per information word and counteracting the reduction of the number of unique bit combinations.

According to a first aspect of the invention this object is achieved with a method as defined in the opening paragraph, characterized in that the code words are spread

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over at least one group of a first type and at least one group of a second type, while the delivery of each of the code words belonging to the group of the first type establishes a first type of coding state determined by the associated group, the delivery of each of the code words belonging to the group of the second type establishes a second type of coding state determined by the information word associated to the delivered code word and, when one of the code words is assigned to the received information word, this code word is selected from a set of code words that depends on the coding state established when the preceding code word was delivered, while the sets of code words belonging to the coding states of the second type do not have code words in common.

According to a second aspect of the invention, a coding device is characterized in that the device comprises state establishing means for establishing a coding state on the delivery of a code word by the converter, the state establishing means being arranged for establishing a first type of coding state for each of the delivered code words belonging to a group of the first type which state is determined by the associated group, and for establishing a second type of coding state for each of the delivered code words belonging to a group of the second type which state is determined by the information word associated to the delivered code word, and the m-to-n-bit converter comprising means for selecting a code word corresponding to the information word from a selection of code words that depends on the coding state, the sets of code words belonging to the coding states of the second type not containing any code words in common.

In the method and coding device according to the invention the combination of the same code word with code words from disjunct sets of code words (= sets without common code words) establishes various unique bit combinations, so that more than one information word can be uniquely represented by the same code word in combination with the successive code word. The code word from the group of the second type is always followed for that matter by a code word of which it is always possible to establish unambiguously to what set this next code word belongs. It is then possible with the code words from each of the disjunct sets always to establish a sufficient number of unique bit combinations to represent all the information words.

These measures thus provide a possibility of establishing a large number of unique bit combinations with code words having a relatively small number of bits per code word. In the case where the code words are selected to be spread over the sets and groups, so that the number of unique bit combinations exceed the number of different information words, it is possible to use the remaining bit combinations for influencing predetermined

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properties of the modulated signal.

It is alternatively possible to use only as many bit combinations as there are information words. In that case the remaining bit combinations allow specific additional requirements to be made on the code words.

For one or more sets, however, there is a preference to assign a pair of code words from the associated set to each of a number of information words, and then, on conversion, to select either of the available code words from the pair according to a specific criterion so as to influence a specific property of the modulated signal. A method in which this is realised is characterized in that the series of information words is converted according to rules of conversion to the series of code words, so that the corresponding modulated signal presents substantially no frequency components in a low-frequency area in the frequency spectrum and in which the modulated signal is any number of successive bit cells having the same minimum signal value $d+1$ and maximum signal value $k+1$, the sets of code words containing a pair of code words for each one of at least a number of information words, while the low-frequency components in the modulated signal are avoided by making selections of code words from the pairs of code words when the information words are converted.

This embodiment is advantageous in that, despite the reduction of the number of bit cells per information word, the presence of low-frequency components in the modulated signal can be largely avoided.

A further embodiment is characterized in that synchronization (sync) words are inserted into the series of code words, the sync words showing bit patterns that cannot occur in the bit string formed by the code words, while the sync words are used having different bit patterns and the sync word used depends on the coding state, a predetermined coding state being established for the conversion of the next information word after a sync word has been inserted, while the sync words are mutually distinguishable on the basis of the logical values of bits at predetermined bit positions in a manner corresponding to the manner in which the sets of code words belonging to coding states of the second type are mutually distinguishable.

This embodiment is advantageous in that in the case where a code word of the group of the second type is followed by a sync word, an information word is established by a bit combination formed by the code word and sync word similarly to the case where the code word of the group of the second type would be followed by a code word.

The latter embodiment is furthermore advantageous in that a coding state

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is established each time after a sync word has been delivered, so that the constraints imposed on the bit string at the transition from sync word to the next code word can always be satisfied.

The signal obtained by the coding device according to the invention is advantageous in that it can be decoded in an extremely simple manner.

An embodiment for a decoding device by which this is realised is characterized in that the converting means are arranged for converting the information word also in dependence on the logical values of bits in the bit string located at predetermined positions with respect to the code word.

The invention will be further explained with reference to the drawing Figures 1 to 17, in which:

Fig. 1 shows a series of information words, a corresponding series of code words and a modulated signal;

Figs. 2 and 3 show tables in which the relation between the information words and code words is established;

Fig. 4 shows the values of various parameters as they are when a series of information words is converted to a series of code words;

Figs. 5a and 5b show the low-frequency portions of frequency spectra of various signals;

Figs. 6 and 8 show various embodiments for coding devices;

Fig. 7 shows an embodiment for a selection circuit to be used in the coding device shown in Fig. 6;

Fig. 9 shows possible bit patterns of suitable sync words;

Fig. 10 shows an adaptation of the coding device of Fig. 6 for the insertion of sync words;

Fig. 11 shows a decoding device;

Fig. 12 shows a record carrier;

Fig. 13 shows a considerably enlarged portion of the record carrier of Fig. 12;

Fig. 14 shows a recording device;

Fig. 15 shows a reading device;

Fig. 16 shows parts of a modulated signal and its corresponding code words, and

Fig. 17 gives a diagrammatic representation of the spreading of code

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words over groups and sets.

Fig. 1 shows three consecutive m-bit information words, in this case, 8-bit information words referenced 1. The three information words 1 have the respective word values "24", "121" and "34". This series of 3 information words 1 is converted to three consecutive n-bit code words, in this case, 16-bit code words referenced 4. The code words 4 form a bit string of bits having a logical "0" value and bits having a logical "1" value. The conversion of the information words is such that in the bit string the minimum number of bits having a logical "0" value positioned between two bits having a logical "1" value is d and the maximum is k, where d is equal to 2 and k is equal to 10. Such a bit string is often referenced a RLL string (RLL = Run Length Limited) with a dk-constraint. The individual bits of the code words will further be referenced x1, ..., x16, where x1 denotes the first bit (from the left) of the code word and x16 denotes the last bit of the code word.

The bit string formed by the code words 4 is converted to a modulated signal 7 by means of a modulo-2 integration operation. This modulated signal comprises three information signal portions 8 representing the code words 4. The information signal portions comprise bit cells 11 which may have a high signal value H or a low signal value L. The number of bit cells per information signal portion is equal to the number of bits of the associated code word. Each code word bit having a logical "1" value is indicated in the modulated signal 7 by a transition from a bit cell having the high signal value to a bit cell having the low signal value, or *vice versa*. Each code word bit having the logical "0" value is indicated in the modulated signal 7 by the absence of a change of signal value at a bit cell transition.

Furthermore, the frequency spectrum of the modulated signal 7 is required to include substantially no low-frequency components. Worded differently, the modulated signal 7 is to be DC-free.

In the following an embodiment of the method according to the invention by which the modulated signal can be obtained will be described in detail.

First there is a requirement with respect to the code words that within the code words the dk-constraint is satisfied. Fig. 17 diagrammatically shows the set of all the possible code words satisfying said dk-constraint in the zone enclosed by frame 170. The code words are divided into at least a group of a first type and at least a group of a second type. When a code word is delivered from one of the groups of the first type, a coding state is established which exclusively depends on the group of the first type to which the delivered code word belongs. When one of the code words of the group of the first type is delivered, a

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coding state is established which depends both on the group of the first type and on the information word represented by the delivered code word. In the embodiment described herein, two groups of the first type can be distinguished *i.e.* a first group G11 which comprises code words ending in a bits having a logical "0" value, where a is an integer equal to 0 or 1, and a second group G12 of code words ending in b bits having a logical "0" where with b is an integer smaller than or equal to 9 and greater than or equal to 6.

In Fig. 17 the code words belonging to group G11 lie in a frame 171. The code words belonging to group G12 lie in a frame 172.

The coding state established by the first group G11 of the first type will henceforth be referenced S1. The coding state established by the second group G12 of the first type will henceforth be referenced S4. The embodiment to be described here only knows one group of the second type. This group comprises code words ending in c bits having a logical "0" value, where c is an integer greater than or equal to 2 and smaller than or equal to 5. This group will henceforth be referenced group G2. In Fig. 17 the code words of group G2 lie in a frame 173. In the example to be described here, two coding states *i.e.* S2 and S3 can be established by the combination of a code word and associated information word.

When the information words are converted to code words, a code word belonging to a set of code words depending on the coding state is assigned to the information word to be converted. The sets of code words belonging to the coding states S1, S2, S3 and S4 will henceforth be referenced V1, V2, V3 and V4, respectively. The code words of the sets V1, V2, V3 and V4 lie in the frames 174, 175, 176 and 177. The code words in the sets are selected such that each bit string that can be formed by a code word from the group that has established a coding state and an arbitrary code word from the set established by this coding state satisfies the dk-constraint. In the case where the coding state S4 is established by the delivery of the previously delivered code word and the coding state thus denotes that the previous code word ends in a bit string having a logical "0" value greater than or equal to 6 and smaller than or equal to 9, code word set V4 which is established by the coding state S4 is only allowed to comprise code words beginning with a maximum of 1 bit having the logical "0" value. For that matter, code words beginning with a larger number of bits having the logical "0" value will have transitional areas between the previously delivered code word and the code word to be delivered, in which areas the number of successive bits having the logical "0" value will not always be smaller than or equal to 10 and thus not satisfy the dk-constraint. For similar reasons, set V1 comprises only code words beginning with a number of bits having the logical "0" value that is greater than or equal to 2 and smaller than or

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equal to 9.

Sets V2 and V3 of code words belonging to the coding states S2 and S3 contain only code words beginning with a number of bits having a logical "0" value greater than or equal to 0 and smaller than or equal to 5. The code words satisfying this condition are spread over the two sets V2 and V3, so that sets V2 and V3 do not contain any common code words at all. Sets V2 and V3 will be referenced disjunct sets in the following. The spreading of the code words over sets V2 and V3 is preferably such that on the basis of the logical values of a limited number of p bits there can be determined to what set a code word belong. In the example described above, the bit combination x1.x13 is used for this purpose. Code words from set V2 are recognisable from the bit combination x1.x13 = 0.0. Code words from set V3 are then recognisable from the combination x1.x13 which is unequal to 0.0. A distinction is made between code words establishing coding state S1 (group G11) on delivery, code words establishing coding state S2 or S3 (group G2) on delivery, and code words establishing the coding state S4 (group G12) on delivery. Set V1 comprises 138 code words from group G11, 96 code words from group G2 and 22 code words from group G12. It will be evident that the number of different code words in set V1 is smaller than the number of different 8-bit information words.

Since the code words from group G2 are always followed by a code word from set V2 or a code word from set V3, and, in addition, based on the code word following a code word from group G2 there may be established what set this code word belongs to, a code word from group G2 followed by a code word from set V2 can be unequivocally distinguished from the same code word from group G2, but followed by a code word from set V3. Worded differently, when code words are assigned to an information word, each code word from group G2 can be used twice. Each code word from group G2 together with a random code word from set V2 forms a unique bit combination which is inseparable from the bit combination formed by the same code word and a random code word from the same set V3. This means that 138 unique bit combinations (code words) from group G11 can be used for set V1, 22 unique bit combinations (code words) from group G12 and 2*96 unique bit combinations (code words from group G2 combined with subsequent code words) from group G2. This brings the total number of useful unique bit combinations to 352. The number of unique bit combinations formed with the code words from sets V2, V3 and V4 are 352, 351 and 415, respectively.

By way of illustration Fig. 17 shows a code word 178 belonging to group G2. This means that the next code word belongs either to set V2 or set V3. Code word 178

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and the next code word are thus capable of unambiguously establishing two different information words. In Fig. 17 code word 178 followed by a code word from set V2, for example, code word 179, establishes a different information word from the one established by code word 178 followed by a code word from set V3, for example, code word 180. Code word 179 belongs to group G11, resulting in that code word 179 is always followed by a code word from set V1, regardless the information word to be coded next, so that code word 179 is capable of establishing not more than a single information word. The same holds for code word 180. The conversion of information words takes place as follows:

Let us assume that the code word delivered last is code word 178 from group G2, the next code word will then belong either to set V2 or set V3, depending on the information word to be converted. Assuming that this information word establishes code word 179, this means that the next code word will belong to set V1. Which code word from set V1 is used is determined by the information word to be converted. In this example this is code word 181. Code word 181 belongs to group G12, so that the next code word will belong to set V4. Which code word this will be will again be established by the information word to be converted. In this example this is code word 182. Code word 182 belongs to group G2. This means that, depending on the information word corresponding to code word 182, the next code word comes either from set V2 or from set V3. Which of the code words from set V2 or V3 is used depends on the information word to be converted. In this example code word 182 is followed by code word 183. Code word 183 also belongs to group G2, so that, depending on the information word corresponding to code word 183, the next code word will come either from set V2 or V3. Which of the code words in the set is used again depends on the information word to be converted. In this case this is code word 184. In the manner described above any random series of information words can be uniquely converted to a series of code words.

In the foregoing an explanation has been given of the number of available code words extended by a subdivision of code words into groups of a first and a second type which establish a coding state, which coding states *per se* establish a set of code words from which a code word is to be selected for the conversion of a next information word. It is then essential that the sets of code words from which a selection is to be made do not have code words in common in the event of coding states laid down by code words from a group of the second type. As a result, it is possible to assign the same code word from a set of code words to different information words, provided that due care is taken that the code words following this same code word belong to different sets that do not have code words in

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common. It will be obvious to a person skilled in the art that said subdivision of code words into sets and groups for obtaining code words to which more than one information word can be assigned can also be applied to code words having a different random number of bits. Neither is it necessary for the series of code words to satisfy a specific dk-constraint. Other constraints are possible, for example, as described in EP-A 0.319.101 (PHN 12.339).

As explained hereinbefore, a larger number of available unique bit combinations arises from the fact that more than one unique bit combination can be established with code words from the group(s) of the second type (G2). Generally, the subdivision of code words into groups and sets will be selected such that the number of available unique bit combinations is larger than the number of different information words. This surplus of unique bit combinations provides the possibility of imposing additional constraints on the conversion.

One possibility is utilizing only as many available unique bit combinations as there are different information words. In that case the surplus of unique bit combinations allows of imposing specific additional constraints on the code words.

However, it is to be preferred for one or more of the sets to assign a pair formed by two code words from the associated set to each of a number of information words, and then select either of the available code words from the pair according to a certain criterion on conversion, so as to influence a specific property of the modulated signal.

A highly attractive possibility is influencing the low-frequency component in the modulated signal. This influence preferably consists of minimizing the DC components. This may be effected by determining the digital sum value at the end of each information signal portion and selecting such code words when the information is converted, so that the digital sum value determined at the end of each information portion continues to be in the neighbourhood of a certain reference value. This may be effected by assigning to a number of information words a pair of code words which effect different changes of the digital sum value. Preferably, each pair of code words comprises not more than two code words for which the changes of the digital sum values have opposite signs. For a given signal level at the end of the last information signal portion, the code word can then be selected for which the digital sum value will be nearest the reference value once the code word has been delivered.

Another possibility of selecting code words is selecting the code word for which, at the given signal level at the end of the code word delivered last, the sign of the digital sum value change caused by the associated code word will be opposite to that of the

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difference between the digital sum value prior to the delivery of the code word and the reference value. The selection of the code word to be delivered when a selection is possible from two code words having opposite influence on the digital sum value may then be simply made on the basis of the signal value at the end of each information signal portion and the sign of the difference between the digital sum value associated to this end and the reference value.

Fig. 2 shows by way of illustration for each of the sets V1, V2, V3 and V4 a code word assigned to each of the possible information words. In this Figure the first (left) column shows the word values of all possible information words. The second, fourth, sixth and eighth columns show the code words assigned to the information words from the respective sets V1, V2, V3 and V4. The third, fifth, seventh and ninth columns show by way of the respective digits 1, 2, 3 and 4 which of the coding states S1, S2, S3 and S4 are established by the associated code word. In Fig. 2 not more than 256 of the available code words are used for each of the sets V1, V2, V3 and V4. Fig. 3 shows, similarly to Fig. 2, the code words of the sets not shown in the table of Fig. 2 for 88 information words to which a pair of two code words is assigned. The code words represented in Fig. 3 will henceforth be referenced alternative code words. The assigning of code words to the information words is such that the change of the digital sum value caused by the alternative code words is the opposite to the change of the digital sum value caused by the code words of Fig. 2 which are assigned to the word values "0" to "87" inclusive.

It should be noted that all all the sets in Fig. 3 contain equally many code words. It will be obvious to a man of ordinary skill in the art that this is not a necessity. It is equally possible that these sets are not equally large.

Furthermore, there is observed that the assignment of code words to the information words is chosen to be such that the relation between, on the one hand, the combination of a code word and the bits x1 and x13 of the next code word and, on the other hand, the information words, is unique, so that the decoding can exclusively be effected based unpon a received code word and the bits x1 and x13 of the next code word. For the code word assignment this means that if a code word occurs in different sets, the same code words in different sets represent the same information words. For example, the information word having the word value "2" is represented by "00100000000100100" in the sets V0 and V2 shown in Fig. 2 and by "10000000000010010" in the sets V2 and V3.

Needless to observe that it is not necessary that code words from different sets represent the same information words. However, this does mean that the coding state is

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to be recovered on decoding to reconstitute the original information word.

The conversion of a series of information words into a series of code words will be further explained with reference to Fig. 4.

Column IW shows from top to bottom the word values of a series of successive m-bit information words. For each of the information words for which a word value is included in column IW are shown a number of data. The column SW represents the coding state laid down when the code word was delivered, which code word was obtained as a result of the conversion of the preceding information word. This code word will henceforth be referenced preceding code word. The coding state in column SW denotes which of the sets V1, V2, V3 and V4 of code words is to be used for the conversion of the information word. Column LB shows the signal value of the modulated signal at the end of the information signal portion which portion corresponds with the code word obtained when the preceding information word was converted. This signal value will henceforth be referenced running information signal value. In the column D S V the digital sum value is shown which belongs to the running signal value of the modulated signal, the running modulated signal value.

Column CW shows the code words assigned to the information words of column IW according to the columns of Figs. 2 and 3. In the case where a pair of code words is assigned to an information word, the two code words of the pair are shown, the upper code word of the pair corresponding to the table of Fig. 2 and the lower code word of the pair corresponding to the table of Fig. 3. Column dDSV shows the change in the digital sum value caused by the code word, assuming that the running modulated signal value would have had value "H".

Column DSVN shows the new digital sum value for the associated code word as this value would be for the case where the associated code word is delivered. Column L B N represents *via* a logical "1" that the signal value at the beginning and end of the information signal portion belonging to the code word are different. A logical "0" indicates that the signal values at the beginning and end of the associated information signal portion are equal. The signal value at the beginning and end of an information signal portion are different if the associated code word contains an odd number of "1" bits, which corresponds to an odd number of changes of signal levels in the information signal portion. With an even number of "1" bits in the code word, the signal value at the beginning and end of the information signal portion is the same. In the column SWN the coding state is shown which would be established in the case where the relevant code word is delivered.

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Furthermore, column CS shows by an asterisk "*" which code word is actually delivered for the associated information word.

The first (top) word from the series of code words shown in column IW has a word value of "2". Let us assume that the coding state (column SW) is S1 when the conversion of the series of information words is initiated, and that the modulated signal begins with the signal level H and that the digital sum value D S V is equal to 0. In that case the associated DSVN value is equal to -6 for the upper code word, whereas the DSVN value is +10 for the lower code word of the pair. When the criterion is applied that the code word is delivered for which the DSVN value is nearest possible a reference value of 0, the upper of the two code words of the pair is delivered for the information word having the word value of "2". This means that the coding state for the next information word (word value "8") becomes S2. At the end of the information signal portion corresponding to the delivered code word, the signal value is L and the signal value at the beginning of the next information portion is thus L as is shown in column LB. The value of dDSV for the upper code word of the pair belonging to the information word having the word value of "8" is equal to -6. This value of -6 applies to the case where the signal value at the beginning of the associated information signal portion would be H. Since this signal value is L in the situation shown, the change of the digital sum value caused by the code word is not equal to -6, but +6. This means that DSVN becomes equal to 0. For the lower code word of the pair DSVN is equal to -18. The value of DSVN for the upper code word is nearest the value of 0, so that the upper code word is delivered. Subsequently, the information word having the word value of "100" is to be converted. Not more than one code word is assigned to this information word, so that a selection depending on DSVN is impossible for this information word. Similarly to the manner described above, the information words having the word values "230", "0", "61" and "255" are converted. Each time a conversion is to take place of an information word to which a pair of code words is assigned, that particular code word is selected from the pair for which the value of DSVN is nearest zero. In this manner the DC voltage level of the modulated signal is maintained at a substantially constant level and the frequency spectrum of the modulated signal will not show any low-frequency components. Although a set of code words is not available for each information word, an influencing of the digital sum value will nevertheless be possible for 88/256 of all the information words to be converted on average. In practice this appears to be amply sufficient to provide that the low-frequency component is absent in the modulated signal. It is to be preferred to include in the code word pairs those code words for which the change caused in the digital sum value is greatest. On the one

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hand, this is advantageous in that the digital sum value can be changed to its maximum. On the other hand, this means that the change caused in the digital sum value is relatively small for code words not belonging to the pair and that the influence of these code words on the digital sum value is relatively small.

By way of illustration Fig. 5a shows the low-frequency portion of the frequency spectrum of a modulated signal obtained by implementing the method according to the invention. In Fig. 5b the corresponding low-frequency portion of the frequency spectrum of an EFM-modulated signal is plotted. As appears from the Figs. 5a and 5b, the frequency spectra for the two signals are substantially the same. The dk-constraint for the EFM-modulated signal and the modulated signal obtained by implementing the method according to the invention is also substantially the same. The number of bit cells per information word in an EFM-modulated signal is equal to 17, whereas this is equal to 16 in a modulated signal according to the invention. This means that if the method according to the invention is implemented, an increase of information density of about 7% is obtained relative to an EFM-modulated signal, without this being at the cost of an increase of the low-frequency contents and without any concessions to the dk-constraint.

Fig. 6 shows an embodiment for a coding device 140 according to the invention by which the method described above can be carried out. The coding device is arranged for converting the m-bit information words 1 to the n-bit code words 4 and the number of different coding states can be indicated by s bits. The coding device comprises a converter 60 for converting (m+s+1) binary input signals to (n+s+t) binary output signals. From the inputs of the converter m inputs are connected to a bus 61 for receiving m-bit information words. From the outputs of the converter n outputs are connected to a bus 62 for delivering n-bit code words. Furthermore, s inputs are connected to an s-bit bus 63 for receiving a state word denoting the current coding state. A state word is delivered by a buffer memory 64, for example, in the form of s flip-flops. The buffer memory 64 has s inputs connected to a bus 58 for receiving a state word to be stored in the buffer memory. For delivering the state words to be stored in the buffer memory, s outputs of the converter 60 are used which are connected to bus 58.

Bus 62 is connected to the parallel inputs of a parallel-to-serial converter 66 which converts code words 4 received over bus 62 to a serial bit string to be supplied over a signal line 67 to a modulator circuit 68 which converts the bit string to the modulated signal 7 to be delivered over signal line 70. The modulator circuit 68 may be one of a customary type, for example, a so-termed modulo-2 integrator.

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In addition to the code words and state words, the converter applies to a bus 75 for each received combination of information word and state word information which

- denotes whether for the associated state word the code word or a pair of code words is assigned to the associated information word,
- denotes for each of these assigned code words the change dDSV of the digital sum value caused by the code word as this change would be for a high signal value at the beginning of an information signal portion corresponding to this code word,
- denotes whether the number of "1" bits in the code word is odd or even.

For information transfer to a selection circuit 76 the bus 75 is connected to inputs of the selection circuit 76.

Based on this information the selection circuit 76 delivers a selection signal which indicates whether the code word to be fed to the bus 62 with the presented information word is to be converted in accordance with the relations laid down in the tables of Fig. 2, or in accordance with the relations laid down in the tables of Fig. 3. This selection signal is applied to the converter 60 over a signal line 77.

The converter 60 may comprise a ROM memory in which the code word tables shown in Figs. 2 and 3 are stored at addresses determined by the combination of state word and information word applied to the inputs of the converter. In response to the detection signal, the addresses of the memory locations are selected with the code words corresponding to the table shown in Fig. 2 or the addresses of the memory locations with the code words corresponding to the table shown in Fig. 3.

In the embodiment shown in Fig. 6 the state words are stored in memory 60. Alternatively, it is possible to derive, by a gate circuit, only the state words from the code words delivered to the bus 62.

Instead of comprising a ROM memory, the converter may also comprise a combinatorial logical circuit formed by gate circuits. The synchronization of the operations executed in the arrangement may be obtained in customary fashion with synchronized clock signals which can be derived by a customary (not shown) clock generating circuit. Fig. 7 shows a possible embodiment for the selection circuit 76. Signal lines forming the bus 75 are split up into a sub-bus 80 and a sub-bus 81. The value of dDSV is transferred over sub-bus 80 for a code word from the table shown in Fig. 2 that is assigned in response to the received combination of state word and information word. Over sub-bus 81 is transferred the value of dDSV for the code word from the table shown in Fig. 3 in the case where this table

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contains a code word for the associated combination of state word and information word. Sub-bus 80 is connected to a first input of an arithmetic circuit 82. A second input of the arithmetic circuit 82 receives, over a bus 85, the value of D S V stored in a buffer memory 83. Furthermore, a control input of the arithmetic circuit receives a control signal over a signal line 84, which signal indicates whether the signal value at the beginning of the information signal portion corresponding to the associated code word has the high value H or the low value L. The signal on signal line 84 is obtained by means of, for example, a flip-flop whose state is constantly adapted when a code word is delivered, which adaptation takes place in response to a signal denoting whether the number of bits having a logical "1" value in the delivered code word is odd or even. This signal is delivered by the converter 60 and supplied over one of the signal lines forming the bus 75. The arithmetic circuit 82 is one of a customary type subtracting or adding the value dDSV received over bus 80 from or to respectively, the value of D S V received over bus 85 in response to the control signal.

The selection circuit 76 comprises a further arithmetic circuit 86 which, similarly to the arithmetic circuit 82, adds the value of dDSV received over bus 81 to the value of D S V received over bus 85 or subtracts it therefrom in response to the control signal on signal line 84. The results of the operations performed by the arithmetic circuits 82 and 86 are applied over a bus 87, 88 respectively, to a decision circuit 89 and a multiplex circuit 90. These results represent, if a code word pair has been assigned to the presented state word, the new digital sum value changes DSVN that would be obtained on delivery of the two different code words of the pair. The decision circuit 89 is of a customary type which determines, in response to the values of DSVN received over the buses 87 and 88, which of the two received values is nearest a reference value, and which circuit 89 feeds a decision signal corresponding to this result to a signal line 91. In the event of a choice from two code words from a pair of code words, the decision signal indicates which of the two code words is to be delivered. This decision signal is applied to the signal line 77 through an AND-gate 92. In the case where not a pair of code words but only one code word is available, the signal on signal line 77 is to indicate that the information word delivered in accordance with the tables as shown in Fig. 2 is to be converted. To realise this, a second input of the AND-gate 92 is supplied with a signal coming from bus 75 which signal indicates whether not more than a single code word or a code word pair is available for the presented combination of state word and information word.

The signal line 77 is also connected to a control input of the multiplex circuit 90. Depending on the signal on its control input the multiplex circuit 90 passes the

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values of DSVN received over buses 87 and 88 on to an output belonging to the delivered code word. The output of the multiplex circuit 90 is coupled to the input of the buffer memory 83. The loading of the buffer memory is controlled in a customary fashion, so that the value of DSVN passed on by the multiplex circuit is stored in the buffer memory 83 when the selected code word is delivered.

In the case where a set of code words is available for a presented information word in said embodiment for the coding device, the code word is selected from the pair for which the digital sum value is nearest a predetermined reference value when the associated code word is delivered. Another possibility of selecting code words from the code word pair is selecting that code word for which the sign of the digital sum value change, which change is caused by the delivery of the code word, is opposite to the sign of the digital sum value at the beginning of the delivery of the code word.

Fig. 8 shows an embodiment for a coding device according to the invention in which the code words are selected on the basis of said criterion. The coding device is again arranged for converting the m-bit information words 1 to the n-bit code words 4, while the number of different coding states can be represented by s bits. The coding device comprises a converter 50 for converting (m+s+1) binary input signals to (n+s) binary output signals. From the inputs of the converter m inputs are connected to a bus 51 for receiving m-bit information words. From the outputs of the converter n outputs are connected to a bus 52 for delivering n-bit code words. Furthermore, s inputs are connected to an s-bit bus 53 for receiving a state word that indicates the instantaneous coding state. The state word is delivered by a buffer memory comprising, for example, s flip-flops. The buffer memory 54 has s inputs connected to a bus for receiving a state word to be loaded in the buffer memory. For delivering the state words to be loaded in the buffer memory, s outputs of the converter 50 are used.

Bus 52 is connected to the parallel inputs of a parallel/serial converter 56 which converts the code words supplied over bus 52 to a serial bit string to be applied, over a signal line 57, to a modulator circuit 58 which converts the bit string to the modulated signal 7 to be delivered over a signal line 40. The modulator circuit 58 may be one of a customary type, for example, a modulo-2 integrator. The modulated signal 7 is applied to a circuit of a customary type for deriving the running digital sum value of the modulated signal 7. Circuit 59 delivers a signal Sdsv which depends on the determined digital sum value, which signal Sdsv denotes whether a code word is to be converted according to the relations laid down in Fig. 2 or a presented information word is to be converted according to the

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relations laid down in Fig. 3. The converter 50 may be of a similar type to converter 60 except for the fact that in the converter 50 only the code words and the associated state words need to be stored. The information supplied to the decision circuit 76 by the converter 60 over bus 75 is redundant in the embodiment shown in Fig. 8.

For the purpose of synchronization of the operations to be performed, the device comprises a clock generating circuit 41 of a customary type generating clock signals for controlling the parallel/serial converter 58 and for controlling the loading of the buffer memory 54.

Preferably, the modulated signal 7 comprises sync signal portions which have a signal pattern that cannot occur in a random sequence of information signal portions. The addition may be effected by inserting sync words into the sequence of n-bit code words. Fig. 9 shows two 26-bit sync words 100 and 101 which are pre-eminently suitable for use in combination with the code words shown in Figs. 2 and 3. The sync words contain each two series of 10 bits having a logical "0" value separated by a bit having a logical "1" value. Only the logical value of the bit at the first location in the code word (x1) is different for the two sync words 100 and 101. Which of the two code words is inserted depends on the coding state determined by the code word situated immediately before the inserted sync word. In the case where the coding state S1 is determined, sync word 101 beginning with 3 bits having the logical "0" value is inserted. Since the code words determining the coding state S1 end in 1 bit having a logical "0" value at the most, the dk-constraint with $d = 2$ and $k = 10$ is satisfied when a transition is made from the code word to the sync word.

In the case where the coding state S4 is laid down, sync word 100 is inserted. Since the code words establishing the coding state S4 end in a minimum of 6 and a maximum of 9 bits having the logical "0" value, the dk-constraint with $d = 2$ and $k = 10$ is again satisfied at the transition from the code word to the sync word.

In the case where the coding state S2 is established, the sync word 101 is inserted. In this sync word the bit combination x1.x13 is equal to 0.0. In the case where the coding state S3 is established, the sync word 100 is inserted. In this sync word the bit combination x1.x13 is equal to 1.0. In the sync word following a code word that establishes the coding state S2, this bit combination x1.x13 is always 0.0 and for a sync word following a code word which establishes state S3 the bit combination x1.x13 is always 1.0, so that an associated information word is always unambiguously established on the basis of the code word and the next code word.

The sync words 100 and 101 both end in a bit having the logical "1"

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value, which means that the code word following either of these sync words is to be selected from the set V1 to provide that at the transition from the sync word to the next code word always the dk-constraint with d = 2 and k = 10 is satisfied. This means that the coding state S1 is established with each delivery of a code word.

Fig. 10 shows a modification of the coding device shown in Fig. 6 by which sync words can be inserted in the manner described above. In Fig. 10 like components to those of Fig. 6 are designated like reference characters. The modification relates to a memory 103 having two memory locations which store each either of the two sync words 100 and 101. The memory 103 comprises an addressing circuit for addressing either of the two memory locations in dependence on the state word applied to address inputs of the memory 103 over the bus 63. The sync word in the addressed memory location is applied to a parallel/serial converter 105 over a bus 104. The serial output of the converter 105 is applied to a first input of an electronically operable switching unit 106. The signal line 67 is connected to a second input of the switch unit 106. The coding device is controlled by a control circuit 107 of a customary type which alternately brings the coding device to a first or to a second state. In the first state a predetermined number of information words are converted to code words which are applied in the serial mode to the modulo-2 integrator 68 *via* the switch unit 106. At the transition from the first to the second state, the conversion of information words is interrupted and the sync word determined by the state word is delivered by memory 103 and applied to the modulo-2 integrator 68 *via* the parallel/serial converter 104 and the switch unit. In addition, at the transition from the second to the first state and under the control of the control circuit 107 the buffer memory is loaded with the state word that corresponds to the coding state S1 and, subsequently, the conversion from information words to code words is resumed until the coding device is again brought to the second state by the control circuit 107.

For the insertion of sync words, the coding device shown in Fig. 8 can be adapted in a way similar to the adaptation shown in Fig. 10.

Fig. 11 shows an embodiment for a decoding device 150 according to the invention for reconverting modulated signals obtained with one of the methods described above to a sequence of information words. The decoding circuit comprises a modulo-2 differentiator 110 for converting the modulated signal to a bit string in which a bit having a logical "1" value represents a transition from a bit cell having a signal value L to a bit cell having a signal value H or *vice versa* and in which each bit cell having the logical "0" value represents two successive bit cells having the same signal value. The bit string thus obtained

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is applied to two series-connected shift registers having each a length corresponding to the length of an n-bit code word. The contents of the shift registers 111 and 112 are supplied to the respective buses 113 and 114 through parallel outputs. The decoding device comprises an (n+p)-to-m-bit converter 115. All the n bits present in shift register 112 are applied to inputs of converter 115 over bus 114. From the n bits present in the shift register 111, p bits are applied to the converter 115 which p bits, together with the n bits in the shift register 114, uniquely establish an information word. The converter 115 may comprise a memory with a look-up table which contains an m-bit information word for each permitted bit combination formed by the n bits of an n-bit code word and the predetermined p bits of a bit string part following this code word. The converter, however, may also be realised by gate circuits.

The conversions performed by the converter 115 may be synchronized in customary fashion by means of a synchronizing circuit 117, so that each time a complete code word is loaded in the shift register 112, the information word is presented on the outputs of the converter which information word corresponds to the bit combination applied to the inputs of the converter 115.

Preferably, a sync word detector 116 connected to buses 113 and 114 and which detects a bit pattern corresponding to the sync words is used for the synchronization.

By way of illustration, Fig. 16 shows a signal that may be obtained in accordance with the invented method described above. The signal comprises a sequence of q successive information signal portions 160, where q is an integer, which signal portions represent q information words. Between the information signal portions are inserted sync signal portions, one of which being designated 161 in Fig. 16. A number of information signal portions are shown in detail. Each of the information signal portions 160 comprises n bit cells, in this case 16, which have a first (low) signal value L or a second (high) signal value H. Since the bit string formed by the code words and represented by the modulated signal satisfies a dk-constraint, the number of successive bit cells having the same signal value will at least be equal to d+1 and at most be equal to k+1. Due to the selection of the code words which depends on the digital sum value, the running value of the difference between the number of bit cells having the first signal value and the bit cells having the second signal value at an arbitrary point in the signal is essentially constant in the signal portion preceding this point. Each information signal portion corresponding to a code word from a group of the first type uniquely establishes an information word. In Fig. 16 this is, for example, information signal portion 160c which corresponds to code word "0100000001000010". This code word uniquely establishes the information word having the

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word value "121". Each information signal portion representing a code word from the group of the second type uniquely represents, together with an adjacent signal portion, an information word.

The information signal portion 160a shown in Fig. 16 corresponds to the code word "00010000000100100". This code word may establish both the information word having the word value "24" and the information word having the word value "34". What information is actually established by this code word is determined by the logical values on the first and thirteenth bit location of the immediately following portion of the bit string. If the logical values of these bits are both equal to 0, the information word having the word value "24" is established. If these bits are unequal to "0", the information word having the word value "34" is established. In Fig. 16 the values of the bits on the first and thirteenth locations behind the code word established by the information signal portion 160a are both equal to "0", so that the information word having the word value "24" is established. The code word established by the information signal portion 160b is identical with the code word established by the information signal portion 160a. The code word represented by the information signal portion 160b, however, is immediately followed by a sync word of which the first bit has the logical "1" value, so that now the information word having the word value "34" is established.

Fig. 12 shows by way of example, a record carrier 120 according to the invention. The record carrier shown is one of an optically detectable type. The record carrier may also be of a different type, for example, of a magnetically readable type. The record carrier comprises information patterns arranged in tracks 121. Fig. 13 shows a strongly enlarged portion 122 of one of the tracks 121. The information pattern in the track portion 121 shown in Fig. 13 comprises first sections 123, for example, in the form of optically detectable marks and second sections 124, for example, intermediate areas lying between the marks. The first and second sections alternate in a direction of the track 125. The first sections 123 present first detectable properties and the second sections 124 present second properties which are distinguishable from the first detectable properties. The first sections 123 represent bit cells 12 of the modulated binary signal 7 having one signal level, for example, the low signal level L. The second sections 124 represent bit cells 11 having the other signal level, for example, the high signal level H. The record carrier 12 may be obtained by first generating the modulated signal and then providing the record carrier with the information pattern. If the record carrier is of an optically detectable type, the record carrier can then be obtained with mastering and replica techniques known *per se* based on the

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modulated signal 7.

Fig. 14 shows a recording device for recording information, in which the coding device according to the invention is used, for example, the coding device 140 shown in Fig. 6. In the recording device the signal line for delivering the modulated signal is connected to a control circuit 141 for a write head 142 along which a record carrier 143 of a writable type is moved. The write head 142 is of a customary type capable of introducing marks having detectable changes on the record carrier 143. The control circuit 141 may also be of a customary type generating a control signal for the write head in response to the modulated signal applied to the control circuit 141, so that the write head 142 introduces a pattern of marks that corresponds to the modulated signal.

Fig. 15 shows a reading device in which a decoding device according to the invention is used, for example, the decoding device 153 shown in Fig. 11. The reading device comprises a read head of a customary type for reading a record carrier according to the invention which record carrier carries an information pattern that corresponds to the modulated signal. The read head 150 then produces an analog read signal modulated according to the information pattern read out by the read head 150. Detection circuit 152 converts this read signal in customary fashion to a binary signal which is applied to the decoding circuit 153.

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CLAIMS:

1. Method of converting a series of m-bit information words to a modulated signal, with m being an integer, in which method an n-bit code word is delivered for each received information word, with n being an integer exceeding m, and the delivered code words are converted to the modulated signal, and in which the series of information words is converted to a series of code words according to rules of conversion, so that the corresponding modulated signal satisfies a predetermined criterion, characterized in that the code words are spread over at least a group of a first type and at least a group of a second type, while the delivery of each of the code words belonging to the group of the first type establishes a first type of coding state determined by the associated group, the delivery of each of the code words belonging to the group of the second type establishes a second type of coding state determined by the information word associated to the delivered code word and, when one of the code words is assigned to the received information word, this code word is selected from a set of code words that depends on the coding state established when the preceding code word was delivered, while the sets of code words belonging to the coding states of the second type do not contain any code words in common.

2. Method as claimed in Claim 1, characterized in that the sequence of information words is converted to the sequence of code words according to such rules of conversion that the corresponding modulated signal presents substantially no frequency components in a low-frequency area in the frequency spectrum and in which each number of successive bit cells having a same signal value in the modulated signal is at least $d+1$ and at most $k+1$, the sets of code words for each of at least a number of information words comprising at least a pair of code words, low-frequency components in the modulated signal being avoided when the information words are converted by selected code words from the pairs of codewords.

3. Method as claimed in Claim 2, characterized in that a running digital sum value is established as a measure for current DC contents, which value is determined over a preceding portion of the modulated signal and denotes for this portion the current value of a difference between the number of bit cells having a first value and the number of bit cells having a second value, while the pairs comprising two code words have opposite effects on

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the digital sum value and the code words are selected from the pairs in response to certain digital sum values so that the digital sum value continues to be limited.

4. Method as claimed in Claim 2 or 3, characterized in that the information words are converted to a sequence of code words which establish a bit string having bits of a first logical value and bits of a second logical value, a number of successive bits having the first logical value and situated among bits having the second logical value being at least d and at most k, and the bit string being converted to the modulated signal, in which transitions from bit cells having the first signal value to bit cells having the second signal value or *vice versa* correspond to the bits having the second logical value in the bit string.

5. Method as claimed in one of the preceding Claims, characterized in that the sets of code words belonging to the coding states of the second type can be mutually distinguished on the basis of the logical values of bits at p predetermined bit positions in the code words, where p is an integer smaller than n.

6. Method as claimed in Claim 5, characterized in that the synchronization (sync) words are inserted into the series of code words, the sync words showing bit patterns that cannot occur in the bit string formed by the code words, while the sync words are used having different bit patterns and the sync word used depends on the coding state, in that a predetermined coding state is established for the conversion of the next information word after a sync word has been inserted, while the sync words are mutually distinguishable on the basis of the logical values of bits at predetermined bit positions in a manner corresponding to the manner in which the sets of code words belonging to coding states of the second type are mutually distinguishable.

7. Method as claimed in one of the preceding Claims, characterized in that d is equal to 2 and k is equal to 10 and in that the ratio of n to m is 2:1.

8. Method as claimed in Claim 7, characterized in that m is equal to 8 and n is equal to 16.

9. Method as claimed in one of the preceding Claims 4, 5, 6, 7, or 8, characterized in that p is equal to 2.

10. Method as claimed in Claim 6, 7, 8, or 9, characterized in that a first group of the second type of code words is formed by code words ending in a bits having the first logical value, where a is equal to 0 or 1, in that a second group of the second type of code words is formed by code words ending in b successive bits having the first logical value, where b is an integer greater than or equal to 6 and smaller than or equal to 9, the group of the second type being formed by code words ending in c bits having the first logical

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value, where c is an integer greater than or equal to 2 and smaller than or equal to 5, and the coding state related sets of code words from which the codewords assigned to the information words are selected are formed by code words beginning with a number of bits of the first logical value, which number of bits depends on the coding state related to the set, so that the number of successive bits having the first logical value in the bit string formed by two successive code words is at least equal to d and at most equal to k.

11. Method for manufacturing a record carrier in which a modulated signal is generated by the method as claimed in one of the preceding Claims and the record carrier is then provided with an information pattern representing this signal.

12. Coding device for performing the method as claimed, the device comprising an m-to-n bit converter for converting the m-bit information words to n-bit code words, and means for converting the n-bit code words to a modulated signal, characterized in that the device comprises state establishing means for establishing a coding state on the delivery of a code word by the converter, the state establishing means being arranged for establishing a first type of coding state for each of the delivered code words belonging to a group of the first type which state is determined by the associated group, and for establishing a second type of coding state for each of the delivered code words belonging to a group of the second type which state is determined by the information word associated to the delivered code word, and the m-to-n-bit converter comprising means for selecting a code word corresponding to the information word from a selection of code words that depends on the coding state, the sets of code words belonging to the coding states of the second type containing no code words in common.

13. Device as claimed in Claim 12 for converting the series of information words to a modulated signal that presents substantially no frequency components in a low-frequency area in the frequency spectrum and wherein each minimum number of successive bit cells having the same signal value is $d+1$ and each maximum number $k+1$, the converter comprising means for generating a pair of code words for each of at least a number of information words and the device comprising selecting means for selecting, for the code word delivery, either of the code words from the pairs in accordance with a predetermined criterion related to the low-frequency contents of the modulated signal.

14. Device as claimed in Claim 13, characterized in that the device comprises means for determining a running digital sum value which value denotes for a preceding part of the modulated signal the running value of a difference between the number of bit cells having a first value and the number of bit cells having a second value, the pairs of code

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words comprising each at least two code words having opposite effects on the digital sum value, and the selecting means comprising means for selecting, according to a criterion depending on the digital sum value, those code words from the sets for which the digital sum value according to this criterion continues to be limited.

15. Device as claimed in Claim 13 or 14, characterized in that the device is arranged for converting information words to a series of code words which establish a bit string of bits having a first logical value and bits having a second logical value, the minimum number of successive bits having the first logical value located between bits having the second logical value being d and the maximum number being k, the device further including a modulo-2 integrator for converting the bit string to the modulated signal.

16. Device as claimed in one of the Claims 12, 14 or 15, characterized in that the sets of code words belonging to the coding states of the second type can be mutually distinguished on the basis of the logical values of bits at p predetermined bit positions in the code words, where p is an integer smaller than or equal to n.

17. Device as claimed in Claim 15 or 16, characterized in that the device comprises means for inserting sync words into the bit string, the sync words displaying bit patterns that cannot occur in the bit string formed by the code words, the device comprising means for selecting sync words to be inserted which have different bit patterns in dependence on the determined coding state, the sync words being mutually distinguishable on the basis of the logical values of bits at predetermined bit positions in a manner that corresponds to the manner in which the sets of code words belonging to the coding states of the second type can be mutually distinguished.

18. Device as claimed in Claim 17, characterized in that the device comprises means for effecting a predetermined coding state once a sync word has been inserted.

19. Device as claimed in one of the Claims 12 to 18, characterized in that d is equal to 2 and k is equal to 10 and in that the ratio of n to m is 2:1.

20. Device as claimed in Claim 19, characterized in that m is equal to 8 and n is equal to 16.

21. Device as claimed in one of the Claims 16 to 20, characterized in that p is equal to 2.

22. Device as claimed in one of the Claims 19, 20 or 21, characterized in that a first group of the second type of code words is formed by code words ending in a bits having the first logical value, where a is equal to 0 or 1, in that a second group of the second type of code words is formed by code words ending in b successive bits having the

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first logical value, where b is an integer greater than or equal to 6 and smaller than or equal to 9, the group of the second type being formed by code words ending in c bits having the first logical value, where c is an integer greater than or equal to 2 and smaller than or equal to 5, and the coding state related sets of code words from which the codewords assigned to the information words are selected are formed by code words beginning with a number of bits of the first logical value, which number of bits depends on the coding state related to the set, so that the number of successive bits having the first logical value in the bit string formed by two successive code words is at least equal to d and at most equal to k.

23. Device for recording information, which device comprises a coding device as claimed in one of the Claims 10 to 12 for converting a series of information words representing the information to a modulated signal and means for recording on a record carrier an information pattern corresponding to the signal.

24. Signal comprising a sequence of q successive information signal portions which represent q information words, where q is an integer, in which signal each of the information signal portions comprises n bit cells having a first or second logical value, each information portion belonging to a predetermined group of information portions uniquely establishing an information word, characterized in that each information signal portion belonging to a second group of information signal portions establishes in combination with an adjacent information signal portion a unique information word.

25. Signal as claimed in Claim 24, characterized in that each number of successive bit cells having the same signal value is minimum d+1 and maximum k+1, and at any arbitrary point in the signal the running value of the difference between the number of bit cells having the first logical value and the bit cells having the seoond logical value in the signal portion preceding this point is limited.

26. Signal as claimed in Claim 25, characterized in that n is equal to 16, d is equal to 2 and k is equal to 10.

27. Signal as claimed in Claim 24, 25 or 26, characterized in that the signal comprises sync signal portions which have bit cell patterns that do not occur in the sequence of successive information signal portions, while a unique information word is established by each of the information signal portions of the second group combined with either an adjacent sync word or an adjacent information signal.

28. Signal as claimed in Claim 24, 25, 26 or 27, characterized in that the presence or absence of changes of the logical value between pairs of successive bit cells at p predetermined bit cell transitions in each of the adjacent signal portions in combination with

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the associated information portion from the second group of information signal portions establish the associated information word, where p is an integer smaller than n.

29. Signal as claimed in Claim 28, characterized in that p is equal to 2.

30. Signal as claimed in one of the Claims 24 to 29, characterized in that the information signal portions end in s bit cells having a same logical value, and in that the information signal portions from the second group end in t bit cells having the same logical value, where s can assume a number of different values and where t can assume a number of different values and where s and t are different.

31. Signal as claimed in Claim 30, characterized in that s is greater than or equal to 2 and smaller than or equal to 5.

32. Record carrier on which the signal as claimed in one of the Claims 24 to 31 is recorded in a track in which information patterns represent the signal portions, which information patterns comprise first and second parts alternating in the direction of the track, the first parts present detectable properties and the second parts present second properties distinguishable from the first properties, and the parts having the first properties represent bit cells having the first logical value and the parts having the second properties represent the bit cells having the second logical value.

33. Decoding device for converting the signal as claimed in one of the Claims 24 to 31 to a series of m-bit information words, this device comprising means for converting the signal to a bit string of bits having a first or second logical value, this bit string containing n-bit code words which correspond to the information signal portions and which device comprises converting means for converting the series of code words to a series of information words, an information word being assigned to each of the code words to be converted and in dependence thereon, characterized in that the converting means are arranged for converting the information word also in dependence on the logical values of bits in the bit string which are located at p predetermined positions relative to the codeword.

34. Decoding device as claimed in Claim 33, characterized in that n is equal to 16 and m is equal to 8, and where p is equal to 2.

35. Decoding device as claimed in Claim 34, characterized in that the p predetermined bit positions are the first and thirteenth bit position past the end of the associated code word.

36. Decoding device as claimed in one of the Claims 33 to 35, characterized in that the device comprises detection means for detecting sync words having bit patterns that cannot be formed by the successive code words in the series, or by a part of the sync word

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in combination with an adjacent code word.

37. Decoding device as claimed in Claim 36, characterized in that the detection means are arranged for detecting 26-bit sync words corresponding to a bit pattern of "10010000000000100000000001" or to a bit pattern of "00010000000000100000000001", where "0" represents a first logical value and where "1" represents a second logical value.

38. Reading device for reading a record carrier on which information is recorded in an information pattern, this device comprising means for converting the information pattern to a corresponding binary reading signal, the reading device comprising a decoding device as claimed in one of the Claims 34 to 39 for converting the binary reading signal to a series of m-bit information words.

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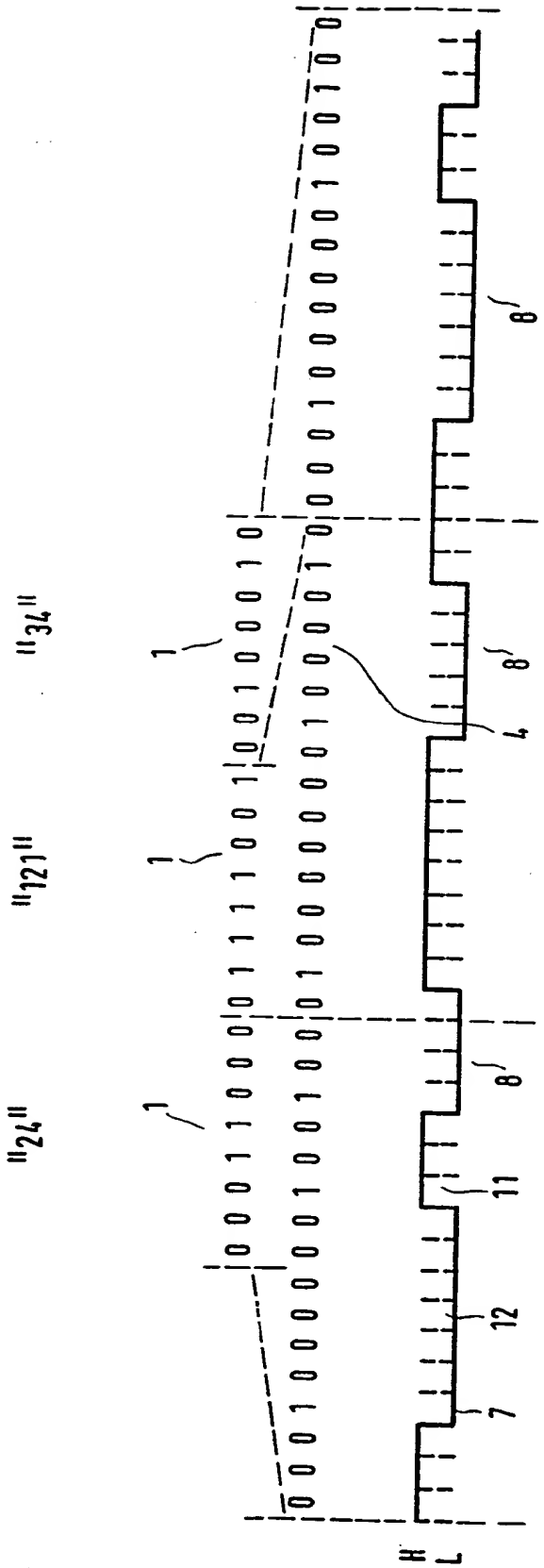



FIG.1

BNSDOCID: <WO__9522802A2_I_>

| | V1 | | V2 | | V3 | | V4 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0010000000001001 | 1 | 0100000000100100 | 2 | 0010000000001001 | 1 | 0100000000100100 | 2 |
| 1 | 0010000000010010 | 1 | 0010000000010010 | 1 | 1000000000100100 | 3 | 1000000000100100 | 3 |
| 2 | 0010000000100100 | 2 | 0010000000100100 | 2 | 1000000000010010 | 1 | 1000000000010010 | 1 |
| 3 | 0010000001001000 | 2 | 0100010010000000 | 4 | 0010000001001000 | 2 | 0100010010000000 | 4 |
| 4 | 0010000010010000 | 2 | 0010000010010000 | 2 | 1000000000100100 | 2 | 1000000000100100 | 2 |
| 5 | 0010000100100000 | 2 | 0010000100100000 | 2 | 1000010010000000 | 4 | 1000010010000000 | 4 |
| 6 | 0010000000100100 | 3 | 0010000000100100 | 3 | 1000100100000000 | 4 | 1000100100000000 | 4 |
| 7 | 0010000001001000 | 3 | 0100000000010010 | 1 | 0010000001001000 | 3 | 0100000000010010 | 1 |
| 8 | 0010000010010000 | 3 | 0010000010010000 | 3 | 1001001000000000 | 4 | 1001001000000000 | 4 |
| 9 | 0010000100100000 | 3 | 0010000100100000 | 3 | 1000000000010001 | 1 | 1000000000010001 | 1 |
| 10 | 0010001001000000 | 4 | 0010001001000000 | 4 | 1000000000100010 | 1 | 1000000000100010 | 1 |
| 11 | 0010010010000000 | 4 | 0010010010000000 | 4 | 0100000001001000 | 3 | 0100000001001000 | 3 |
| 12 | 0000010000000001 | 1 | 0000010000000001 | 1 | 0100000001001000 | 2 | 0100000001001000 | 2 |
| 13 | 0000100000000010 | 1 | 0000100000000010 | 1 | 1000010010000001 | 1 | 1000010010000001 | 1 |
| 14 | 0001000000001001 | 1 | 0100000000100100 | 3 | 0001000000001001 | 1 | 0100000000100100 | 3 |
| 15 | 0001000000010010 | 1 | 0001000000010010 | 1 | 1000100100000001 | 1 | 1000100100000001 | 1 |
| 16 | 0010000000010001 | 1 | 0010000000010001 | 1 | 1001001000000001 | 1 | 1001001000000001 | 1 |
| 17 | 0010000000100010 | 1 | 0010000000100010 | 1 | 1000010001000000 | 4 | 1000010001000000 | 4 |
| 18 | 0010000001001001 | 1 | 0100000010010000 | 2 | 0010000001001001 | 1 | 0100000010010000 | 2 |
| 19 | 0010000010010001 | 1 | 0010000010010001 | 1 | 1000100010000000 | 4 | 1000100010000000 | 4 |
| 20 | 0010000100100001 | 1 | 0010000100100001 | 1 | 1001000100000000 | 4 | 1001000100000000 | 4 |
| 21 | 0010001001000001 | 1 | 0010001001000001 | 1 | 0100000001001001 | 1 | 0100000001001001 | 1 |
| 22 | 0010010010000001 | 1 | 0010010010000001 | 1 | 1000000000100001 | 1 | 1000000000100001 | 1 |
| 23 | 0001000000000100 | 2 | 0001000000000100 | 2 | 0100000010001000 | 2 | 0100000010001000 | 2 |
| 24 | 0001000000100100 | 2 | 0001000000100100 | 2 | 0100000010001000 | 3 | 0100000010001000 | 3 |
| 25 | 0001000001001000 | 2 | 0100000100100000 | 2 | 0001000001001000 | 2 | 0100000100100000 | 2 |
| 26 | 0001000010010000 | 2 | 0001000010010000 | 2 | 1000010001000001 | 1 | 1000010001000001 | 1 |
| 27 | 0001000100100000 | 2 | 0001000100100000 | 2 | 1000010010000010 | 1 | 1000010010000010 | 1 |
| 28 | 0010000000001000 | 2 | 0100000010010000 | 3 | 0010000000001000 | 2 | 0100000010010000 | 3 |
| 29 | 0010000001000100 | 2 | 0010000001000100 | 2 | 1000100010000001 | 1 | 1000100010000001 | 1 |
| 30 | 0010000010001000 | 2 | 0100000100100000 | 3 | 0010000010001000 | 2 | 0100000100100000 | 3 |

FIG. 2A

BNSDOCID: <WO__9522802A2_I_>

| | $V_1$ | | $V_2$ | | $V_3$ | | $V_4$ | |
|---|---|---|---|---|---|---|---|---|
| 31 | 0010000100010000 | 2 | 0010000100010000 | 2 | 1000100100000010 | 1 | 1000100100000010 | 1 |
| 32 | 0010001000100000 | 2 | 0010001000100000 | 2 | 1001000100000001 | 1 | 1001000100000001 | 1 |
| 33 | 0001000000000100 | 3 | 0001000000000100 | 3 | 1001001000000010 | 1 | 1001001000000010 | 1 |
| 34 | 0001000000100100 | 3 | 0001000000100100 | 3 | 1000010000100000 | 2 | 1000010000100000 | 2 |
| 35 | 0001000001001000 | 3 | 0100001001000000 | 4 | 0001000001001000 | 3 | 0100001001000000 | 4 |
| 36 | 0001000010010000 | 3 | 0001000010010000 | 3 | 1000010000100000 | 3 | 1000010000100000 | 3 |
| 37 | 0001000100100000 | 3 | 0001000100100000 | 3 | 1000100001000000 | 4 | 1000100001000000 | 4 |
| 38 | 0010000000001000 | 3 | 0100010010000001 | 1 | 0010000000001000 | 3 | 0100010010000001 | 1 |
| 39 | 0010000001000100 | 3 | 0010000001000100 | 3 | 1001000010000000 | 4 | 1001000010000000 | 4 |
| 40 | 0010000010001000 | 3 | 0100000000100010 | 1 | 0010000010001000 | 3 | 0100000000100010 | 1 |
| 41 | 0010000100010000 | 3 | 0010000100010000 | 3 | 0100000010001001 | 1 | 0100000010001001 | 1 |
| 42 | 0010001000100000 | 3 | 0010001000100000 | 3 | 1000000000100000 | 2 | 1000000000100000 | 2 |
| 43 | 0001001001000000 | 4 | 0001001001000000 | 4 | 1000100100001001 | 1 | 1000100100001001 | 1 |
| 44 | 0010010001000000 | 4 | 0010010001000000 | 4 | 0100000100001000 | 3 | 0100000100001000 | 3 |
| 45 | 0000001000000001 | 1 | 0100010001000000 | 4 | 1000001000000001 | 1 | 0100010001000000 | 4 |
| 46 | 0000010000000010 | 1 | 0000010000000010 | 1 | 1000010010001001 | 1 | 1000010010001001 | 1 |
| 47 | 0000100000001001 | 1 | 0100000000010001 | 1 | 0000100000001001 | 1 | 0100000000010001 | 1 |
| 48 | 0000100000010010 | 1 | 0000100000010010 | 1 | 0100000100001000 | 2 | 0100000100001000 | 2 |
| 49 | 0001000000010001 | 1 | 0001000000010001 | 1 | 1001001001001000 | 2 | 1001001001001000 | 2 |
| 50 | 0001000000100010 | 1 | 0001000000100010 | 1 | 1000000000100000 | 3 | 1000000000100000 | 3 |
| 51 | 0001000001001001 | 1 | 0100000010010001 | 1 | 0001000001001001 | 1 | 0100000010010001 | 1 |
| 52 | 0001000010010001 | 1 | 0001000010010001 | 1 | 1000010000100001 | 1 | 1000010000100001 | 1 |
| 53 | 0001000100100001 | 1 | 0001000100100001 | 1 | 1000010001000010 | 1 | 1000010001000010 | 1 |
| 54 | 0001001001000001 | 1 | 0001001001000001 | 1 | 1000010010010010 | 1 | 1000010010010010 | 1 |
| 55 | 0010000000100001 | 1 | 0010000000100001 | 1 | 1000100001000001 | 1 | 1000100001000001 | 1 |
| 56 | 0010000001000010 | 1 | 0010000001000010 | 1 | 1000100010000010 | 1 | 1000100010000010 | 1 |
| 57 | 0010000010001001 | 1 | 0100000100100001 | 1 | 0010000010001001 | 1 | 0100000100100001 | 1 |
| 58 | 0010000010010010 | 1 | 0010000010010010 | 1 | 1000100100010010 | 1 | 1000100100010010 | 1 |
| 59 | 0010000100010001 | 1 | 0010000100010001 | 1 | 1001000010000001 | 1 | 1001000010000001 | 1 |
| 60 | 0010000100100010 | 1 | 0010000100100010 | 1 | 1001000100000010 | 1 | 1001000100000010 | 1 |
| 61 | 0010001000100001 | 1 | 0010001000100001 | 1 | 1001001000010010 | 1 | 1001001000010010 | 1 |

FIG. 2B

BNSDOCID: <WO__9522802A2_1_>

| | $V_1$ | | $V_2$ | | $V_3$ | | $V_4$ | |
|---|---|---|---|---|---|---|---|---|
| 62 | 0010001001000010 | 1 | 0010001001000010 | 1 | 1001001000001001 | 1 | 1001001000001001 | 1 |
| 63 | 0010010001000001 | 1 | 0010010001000001 | 1 | 1000010000010000 | 2 | 1000010000010000 | 2 |
| 64 | 0010010010000010 | 1 | 0010010010000010 | 1 | 1000010010000100 | 2 | 1000010010000100 | 2 |
| 65 | 0000100000000100 | 2 | 0000100000000100 | 2 | 1000100000100000 | 2 | 1000100000100000 | 2 |
| 66 | 0000100000100100 | 2 | 0000100000100100 | 2 | 1000100100000100 | 2 | 1000100100000100 | 2 |
| 67 | 0000100001001000 | 2 | 0100001001000001 | 1 | 0000100001001000 | 2 | 0100001001000001 | 1 |
| 68 | 0000100010010000 | 2 | 0000100010010000 | 2 | 1000100100100100 | 2 | 1000100100100100 | 2 |
| 69 | 0000100100100000 | 2 | 0000100100100000 | 2 | 1001001000000100 | 2 | 1001001000000100 | 2 |
| 70 | 0001000000001000 | 2 | 0100000001000100 | 2 | 0001000000001000 | 2 | 0100000001000100 | 2 |
| 71 | 0001000001000100 | 2 | 0001000001000100 | 2 | 1001001000100100 | 2 | 1001001000100100 | 2 |
| 72 | 0001000010001000 | 2 | 0100000100010000 | 2 | 0001000010001000 | 2 | 0100000100010000 | 2 |
| 73 | 0001000100010000 | 2 | 0001000100010000 | 2 | 1000010000010000 | 3 | 1000010000010000 | 3 |
| 74 | 0001001000100000 | 2 | 0001001000100000 | 2 | 1000010010000100 | 3 | 1000010010000100 | 3 |
| 75 | 0010000000010000 | 2 | 0010000000010000 | 2 | 1000100000100000 | 3 | 1000100000100000 | 3 |
| 76 | 0010000010000100 | 2 | 0010000010000100 | 2 | 1000100100000100 | 3 | 1000100100000100 | 3 |
| 77 | 0010000100001000 | 2 | 0100001000100000 | 2 | 0010000100001000 | 2 | 0100001000100000 | 2 |
| 78 | 0010001000010000 | 2 | 0010001000010000 | 2 | 1000100100100100 | 3 | 1000100100100100 | 3 |
| 79 | 0010010000100000 | 2 | 0010010000100000 | 2 | 1001001000000100 | 3 | 1001001000000100 | 3 |
| 80 | 0000100000000100 | 3 | 0000100000000100 | 3 | 1001001000100100 | 3 | 1001001000100100 | 3 |
| 81 | 0000100000100100 | 3 | 0000100000100100 | 3 | 1001000001000000 | 4 | 1001000001000000 | 4 |
| 82 | 0000100001001000 | 3 | 0100000001000100 | 3 | 0000100001001000 | 3 | 0100000001000100 | 3 |
| 83 | 0000100010010000 | 3 | 0000100010010000 | 3 | 1001001001001000 | 3 | 1001001001001000 | 3 |
| 84 | 0000100100100000 | 3 | 0000100100100000 | 3 | 0100001000001000 | 2 | 0100001000001000 | 2 |
| 85 | 0001000000001000 | 3 | 0100000100010000 | 3 | 0001000000001000 | 3 | 0100000100010000 | 3 |
| 86 | 0001000001000100 | 3 | 0001000001000100 | 3 | 1000010000001000 | 2 | 1000010000001000 | 2 |
| 87 | 0001000010001000 | 3 | 0100001000100000 | 3 | 0001000010001000 | 3 | 0100001000100000 | 3 |
| 88 | 0001000100010000 | 3 | 0001000100010000 | 3 | 1000010000001000 | 3 | 1000010000001000 | 3 |
| 89 | 0001001000100000 | 3 | 0001001000100000 | 3 | 0100000100001001 | 1 | 0100000100001001 | 1 |
| 90 | 0010000000010000 | 3 | 0010000000010000 | 3 | 0100001001001001 | 1 | 0100001001001001 | 1 |
| 91 | 0010000010000100 | 3 | 0010000010000100 | 3 | 0100010010001001 | 1 | 0100010010001001 | 1 |
| 92 | 0010000100001000 | 3 | 0100100100000001 | 1 | 0010000100001000 | 3 | 0100100100000001 | 1 |

FIG. 2c

BNSDOCID: <WO__9522802A2_I_>

BNSDOCID: <WO__9522802A2_I_>





| | $V_1$ | | $V_2$ | | $V_3$ | | $V_4$ | |
|---|---|---|---|---|---|---|---|---|
| 93 | 0010001000010000 | 3 | 0010001000010000 | 3 | 1000100010001001 | 1 | 1000100010001001 | 1 |
| 94 | 0010010000100000 | 3 | 0010010000100000 | 3 | 1001001001001001 | 1 | 1001001001001001 | 1 |
| 95 | 0000000100000001 | 1 | 0100010010000010 | 1 | 1000000100000001 | 1 | 0100010010000010 | 1 |
| 96 | 0000001000000010 | 1 | 0100100010000001 | 1 | 1000001000000010 | 1 | 0100100010000001 | 1 |
| 97 | 0000010000001001 | 1 | 0100000000010000 | 2 | 0000010000001001 | 1 | 0100000000010000 | 2 |
| 98 | 0000010000010010 | 1 | 0000010000010010 | 1 | 1000010010001000 | 2 | 1000010010001000 | 2 |
| 99 | 0000100000010001 | 1 | 0000100000010001 | 1 | 0100001000001000 | 3 | 0100001000001000 | 3 |
| 100 | 0000100000100010 | 1 | 0000100000100010 | 1 | 1000010000010001 | 1 | 1000010000010001 | 1 |
| 101 | 0000100001001001 | 1 | 0100010001000001 | 1 | 0000100001001001 | 1 | 0100010001000001 | 1 |
| 102 | 0000100010010001 | 1 | 0000100010010001 | 1 | 1000010000100010 | 1 | 1000010000100010 | 1 |
| 103 | 0000100100100001 | 1 | 0000100100100001 | 1 | 1000010010010001 | 1 | 1000010010010001 | 1 |
| 104 | 0001000000100001 | 1 | 0001000000100001 | 1 | 1000100000100001 | 1 | 1000100000100001 | 1 |
| 105 | 0001000001000010 | 1 | 0001000001000010 | 1 | 1000100001000010 | 1 | 1000100001000010 | 1 |
| 106 | 0001000010001001 | 1 | 0100010000100000 | 2 | 0001000010001001 | 1 | 0100010000100000 | 2 |
| 107 | 0001000010010010 | 1 | 0001000010010010 | 1 | 1000100010010010 | 1 | 1000100010010010 | 1 |
| 108 | 0001000100010001 | 1 | 0001000100010001 | 1 | 1000100100010001 | 1 | 1000100100010001 | 1 |
| 109 | 0001000100100010 | 1 | 0001000100100010 | 1 | 1000100100100010 | 1 | 1000100100100010 | 1 |
| 110 | 0001001000100001 | 1 | 0001001000100001 | 1 | 1001000001000001 | 1 | 1001000001000001 | 1 |
| 111 | 0001001001000010 | 1 | 0001001001000010 | 1 | 1001000010000010 | 1 | 1001000010000010 | 1 |
| 112 | 0010000001000001 | 1 | 0010000001000001 | 1 | 1001000100010010 | 1 | 1001000100010010 | 1 |
| 113 | 0010000010000010 | 1 | 0010000010000010 | 1 | 1001001000010001 | 1 | 1001001000010001 | 1 |
| 114 | 0010000100001001 | 1 | 0100010000100000 | 3 | 0010000100001001 | 1 | 0100010000100000 | 3 |
| 115 | 0010000100010010 | 1 | 0010000100010010 | 1 | 1001001000100010 | 1 | 1001001000100010 | 1 |
| 116 | 0010001000010001 | 1 | 0010001000010001 | 1 | 0100100100001001 | 1 | 0100100100001001 | 1 |
| 117 | 0010001000100010 | 1 | 0010001000100010 | 1 | 1001000100001001 | 1 | 1001000100001001 | 1 |
| 118 | 0010001001001001 | 1 | 0100000000100001 | 1 | 0010001001001001 | 1 | 0100000000100001 | 1 |
| 119 | 0010010000100001 | 1 | 0010010000100001 | 1 | 1000010001000100 | 2 | 1000010001000100 | 2 |
| 120 | 0010010001000010 | 1 | 0010010001000010 | 1 | 1000100000010000 | 2 | 1000100000010000 | 2 |
| 121 | 0010010010001001 | 1 | 0100000001000010 | 1 | 0010010010001001 | 1 | 0100000001000010 | 1 |
| 122 | 0010010010010010 | 1 | 0010010010010010 | 1 | 1000100010000100 | 2 | 1000100010000100 | 2 |
| 123 | 0000010000000100 | 2 | 0000010000000100 | 2 | 1001000000100000 | 2 | 1001000000100000 | 2 |

FIG. 2D

| | $V_1$ | | $V_2$ | | $V_3$ | | $V_4$ | |
|---|---|---|---|---|---|---|---|---|
| 124 | 0000010000100100 | 2 | 0000010000100100 | 2 | 1001000100000100 | 2 | 1001000100000100 | 2 |
| 125 | 0000010001001000 | 2 | 0100000010010010 | 1 | 0000010001001000 | 2 | 0100000010010010 | 1 |
| 126 | 0000010010010000 | 2 | 0000010010010000 | 2 | 1001000100100100 | 2 | 1001000100100100 | 2 |
| 127 | 0000100000001000 | 2 | 0100000100010001 | 1 | 0000100000001000 | 2 | 0100000100010001 | 1 |
| 128 | 0000100001000100 | 2 | 0000100001000100 | 2 | 1001001001000100 | 2 | 1001001001000100 | 2 |
| 129 | 0000100010001000 | 2 | 0100000100100010 | 1 | 0000100010001000 | 2 | 0100000100100010 | 1 |
| 130 | 0000100100010000 | 2 | 0000100100010000 | 2 | 1000100100001000 | 2 | 1000100100001000 | 2 |
| 131 | 0001000000010000 | 2 | 0001000000010000 | 2 | 1000010001000100 | 3 | 1000010001000100 | 3 |
| 132 | 0001000010000100 | 2 | 0001000010000100 | 2 | 1000100000010000 | 3 | 1000100000010000 | 3 |
| 133 | 0001000100001000 | 2 | 0100001000100001 | 1 | 0001000100001000 | 2 | 0100001000100001 | 1 |
| 134 | 0001001000010000 | 2 | 0001001000010000 | 2 | 1000100010000100 | 3 | 1000100010000100 | 3 |
| 135 | 0010000000100000 | 2 | 0010000000100000 | 2 | 1001000000100000 | 3 | 1001000000100000 | 3 |
| 136 | 0010000100000100 | 2 | 0010000100000100 | 2 | 1001000100000100 | 3 | 1001000100000100 | 3 |
| 137 | 0010000100100100 | 2 | 0010000100100100 | 2 | 1001000100100100 | 3 | 1001000100100100 | 3 |
| 138 | 0010001000001000 | 2 | 0100001001000010 | 1 | 0010001000001000 | 2 | 0100001001000010 | 1 |
| 139 | 0010001001000100 | 2 | 0010001001000100 | 2 | 1001001001000100 | 3 | 1001001001000100 | 3 |
| 140 | 0010010000010000 | 2 | 0010010000010000 | 2 | 1000010001001001 | 1 | 1000010001001001 | 1 |
| 141 | 0010010010000100 | 2 | 0010010010000100 | 2 | 1001001000001000 | 2 | 1001001000001000 | 2 |
| 142 | 0000010000000100 | 3 | 0000010000000100 | 3 | 1000100100001000 | 3 | 1000100100001000 | 3 |
| 143 | 0000010000100100 | 3 | 0000010000100100 | 3 | 1001001000001000 | 3 | 1001001000001000 | 3 |
| 144 | 0000010001001000 | 3 | 0100000010000100 | 2 | 0000010001001000 | 3 | 0100000010000100 | 2 |
| 145 | 0000010010010000 | 3 | 0000010010010000 | 3 | 1000000001000000 | 4 | 1000000001000000 | 4 |
| 146 | 0000100000001000 | 3 | 0100001000010000 | 2 | 0000100000001000 | 3 | 0100001000010000 | 2 |
| 147 | 0000100001000100 | 3 | 0000100001000100 | 3 | 1000010001001000 | 2 | 1000010001001000 | 2 |
| 148 | 0000100010001000 | 3 | 0100000010000100 | 3 | 0000100010001000 | 3 | 0100000010000100 | 3 |
| 149 | 0000100100010000 | 3 | 0000100100010000 | 3 | 0100001001001000 | 3 | 0100001001001000 | 3 |
| 150 | 0001000000010000 | 3 | 0001000000010000 | 3 | 0100010010001000 | 3 | 0100010010001000 | 3 |
| 151 | 0001000010000100 | 3 | 0001000010000100 | 3 | 1000000010000000 | 4 | 1000000010000000 | 4 |
| 152 | 0001000100001000 | 3 | 0100001000010000 | 3 | 0001000100001000 | 3 | 0100001000010000 | 3 |
| 153 | 0001001000010000 | 3 | 0001001000010000 | 3 | 0100001000001001 | 1 | 0100001000001001 | 1 |
| 154 | 0010000000100000 | 3 | 0010000000100000 | 3 | 1000100010001000 | 2 | 1000100010001000 | 2 |

FIG. 2E

BNSDOCID: <WO__9522802A2_1>

| | $V_1$ | | $V_2$ | | $V_3$ | | $V_4$ | |
|---|---|---|---|---|---|---|---|---|
| 155 | 0010000100000100 | 3 | 0010000100000100 | 3 | 0100010000001000 | 3 | 0100010000001000 | 3 |
| 156 | 0010000100100100 | 3 | 0010000100100100 | 3 | 1000100001001001 | 1 | 1000100001001001 | 1 |
| 157 | 0010001000001000 | 3 | 0100100100000010 | 1 | 0010001000001000 | 3 | 0100100100000010 | 1 |
| 158 | 0010001001000100 | 3 | 0010001001000100 | 3 | 1000010010001000 | 3 | 0100100100000000 | 4 |
| 159 | 0010010000010000 | 3 | 0010010000010000 | 3 | 0100001001001000 | 2 | 0100001001001000 | 2 |
| 160 | 0010010010000100 | 3 | 0010010010000100 | 3 | 0100010010001000 | 2 | 0100010010001000 | 2 |
| 161 | 0000000010000001 | 1 | 0100000000010000 | 3 | 1000000010000001 | 1 | 0100000000010000 | 3 |
| 162 | 0000000100000010 | 1 | 0100100000100000 | 2 | 1000000100000010 | 1 | 0100100000100000 | 2 |
| 163 | 0000001000001001 | 1 | 0100100100100100 | 3 | 1000001000001001 | 1 | 0100100100100100 | 3 |
| 164 | 0000001000010010 | 1 | 0100010000100001 | 1 | 1000001000010010 | 1 | 0100010000100001 | 1 |
| 165 | 0000010000010001 | 1 | 0000010000010001 | 1 | 0100100100001000 | 2 | 0100100100001000 | 2 |
| 166 | 0000010000100010 | 1 | 0000010000100010 | 1 | 1001000100001000 | 2 | 1001000100001000 | 2 |
| 167 | 0000010001001001 | 1 | 0100010010000100 | 2 | 0000010001001001 | 1 | 0100010010000100 | 2 |
| 168 | 0000010010010001 | 1 | 0000010010010001 | 1 | 1000100010001000 | 3 | 1000100010001000 | 3 |
| 169 | 0000100000100001 | 1 | 0000100000100001 | 1 | 1000010000010010 | 1 | 1000010000010010 | 1 |
| 170 | 0000100001000010 | 1 | 0000100001000010 | 1 | 1000100000010001 | 1 | 1000100000010001 | 1 |
| 171 | 0000100010001001 | 1 | 0100100000100000 | 3 | 0000100010001001 | 1 | 0100100000100000 | 3 |
| 172 | 0000100010010010 | 1 | 0000100010010010 | 1 | 1000100000100010 | 1 | 1000100000100010 | 1 |
| 173 | 0000100100010001 | 1 | 0000100100010001 | 1 | 1000100010010001 | 1 | 1000100010010001 | 1 |
| 174 | 0000100100100010 | 1 | 0000100100100010 | 1 | 1000100100100001 | 1 | 1000100100100001 | 1 |
| 175 | 0001000001000001 | 1 | 0001000001000001 | 1 | 1001000000100001 | 1 | 1001000000100001 | 1 |
| 176 | 0001000010000010 | 1 | 0001000010000010 | 1 | 1001000001000010 | 1 | 1001000001000010 | 1 |
| 177 | 0001000100001001 | 1 | 0100100001000001 | 1 | 0001000100001001 | 1 | 0100100001000001 | 1 |
| 178 | 0001000100010010 | 1 | 0001000100010010 | 1 | 1001000010010010 | 1 | 1001000010010010 | 1 |
| 179 | 0001001000010001 | 1 | 0001001000010001 | 1 | 1001000100010001 | 1 | 1001000100010001 | 1 |
| 180 | 0001001000100010 | 1 | 0001001000100010 | 1 | 1001000100100010 | 1 | 1001000100100010 | 1 |
| 181 | 0001001001001001 | 1 | 0100010000010000 | 2 | 0001001001001001 | 1 | 0100010000010000 | 2 |
| 182 | 0010000010000001 | 1 | 0010000010000001 | 1 | 1001001000100001 | 1 | 1001001000100001 | 1 |
| 183 | 0010000100000010 | 1 | 0010000100000010 | 1 | 1001001001000010 | 1 | 1001001001000010 | 1 |
| 184 | 0010001000001001 | 1 | 0100010010000100 | 3 | 0010001000001001 | 1 | 0100010010000100 | 3 |
| 185 | 0010001000010010 | 1 | 0010001000010010 | 1 | 1000010000000100 | 2 | 1000010000000100 | 2 |



FIG. 2F

BNSDOCID: <WO_9522802A2_1>

| | $V_1$ | | $V_2$ | | $V_3$ | | $V_4$ | |
|---|---|---|---|---|---|---|---|---|
| 186 | 0010010000010001 | 1 | 0010010000010001 | 1 | 1000010000100100 | 2 | 1000010000100100 | 2 |
| 187 | 0010010000100010 | 1 | 0010010000100010 | 1 | 1000010010010000 | 2 | 1000010010010000 | 2 |
| 188 | 0010010001001001 | 1 | 0100010010010010 | 1 | 0010010001001001 | 1 | 0100010010010010 | 1 |
| 189 | 0010010010010001 | 1 | 0010010010010001 | 1 | 1000100001000100 | 2 | 1000100001000100 | 2 |
| 190 | 0000001000000100 | 2 | 0100000000100000 | 2 | 1000001000000100 | 2 | 0100000000100000 | 2 |
| 191 | 0000001000100100 | 2 | 0100100100000100 | 2 | 1000001000100100 | 2 | 0100100100000100 | 2 |
| 192 | 0000001001001000 | 2 | 0100100100100100 | 2 | 1000001001001000 | 2 | 0100100100100100 | 2 |
| 193 | 0000010000001000 | 2 | 0100010000010000 | 3 | 0000010000001000 | 2 | 0100010000010000 | 3 |
| 194 | 0000010001000100 | 2 | 0000010001000100 | 2 | 1000100100010000 | 2 | 1000100100010000 | 2 |
| 195 | 0000010010001000 | 2 | 0100000001000001 | 1 | 0000010010001000 | 2 | 0100000001000001 | 1 |
| 196 | 0000100000010000 | 2 | 0000100000010000 | 2 | 1001000000010000 | 2 | 1001000000010000 | 2 |
| 197 | 0000100010000100 | 2 | 0000100010000100 | 2 | 1001000010000100 | 2 | 1001000010000100 | 2 |
| 198 | 0000100100001000 | 2 | 0100000010000010 | 1 | 0000100100001000 | 2 | 0100000010000010 | 1 |
| 199 | 0001000000100000 | 2 | 0001000000100000 | 2 | 1001001000010000 | 2 | 1001001000010000 | 2 |
| 200 | 0001000100000100 | 2 | 0001000100000100 | 2 | 1000010000000100 | 3 | 1000010000000100 | 3 |
| 201 | 0001000100100100 | 2 | 0001000100100100 | 2 | 1000010000100100 | 3 | 1000010000100100 | 3 |
| 202 | 0001001000001000 | 2 | 0100000100010010 | 1 | 0001001000001000 | 2 | 0100000100010010 | 1 |
| 203 | 0001001001000100 | 2 | 0001001001000100 | 2 | 1000010010010000 | 3 | 1000010010010000 | 3 |
| 204 | 0010001000000100 | 2 | 0010001000000100 | 2 | 1000100001000100 | 3 | 1000100001000100 | 3 |
| 205 | 0010001000100100 | 2 | 0010001000100100 | 2 | 1000100100010000 | 3 | 1000100100010000 | 3 |
| 206 | 0010001001001000 | 2 | 0100001000010001 | 1 | 0010001001001000 | 2 | 0100001000010001 | 1 |
| 207 | 0010010000001000 | 2 | 0100001000100010 | 1 | 0010010000001000 | 2 | 0100001000100010 | 1 |
| 208 | 0010010001000100 | 2 | 0010010001000100 | 2 | 1001000000010000 | 3 | 1001000000010000 | 3 |
| 209 | 0010010010001000 | 2 | 0100010001000010 | 1 | 0010010010001000 | 2 | 0100010001000010 | 1 |
| 210 | 0000001000000100 | 3 | 0100100010000010 | 1 | 1000001000000100 | 3 | 0100100010000010 | 1 |
| 211 | 0000001000100100 | 3 | 0100000100000100 | 2 | 1000001000100100 | 3 | 0100000100000100 | 2 |
| 212 | 0000001001001000 | 3 | 0100000100100100 | 2 | 1000001001001000 | 3 | 0100000100100100 | 2 |
| 213 | 0000010000001000 | 3 | 0100100100010010 | 1 | 0000010000001000 | 3 | 0100100100010010 | 1 |
| 214 | 0000010001000100 | 3 | 0000010001000100 | 3 | 1001000010000100 | 3 | 1001000010000100 | 3 |
| 215 | 0000010010001000 | 3 | 0100001001000100 | 2 | 0000010010001000 | 3 | 0100001001000100 | 2 |
| 216 | 0000100000010000 | 3 | 0000100000010000 | 3 | 1001001000010000 | 3 | 1001001000010000 | 3 |

FIG. 2G

BNSDOCID: <WO__9522802A2_1>

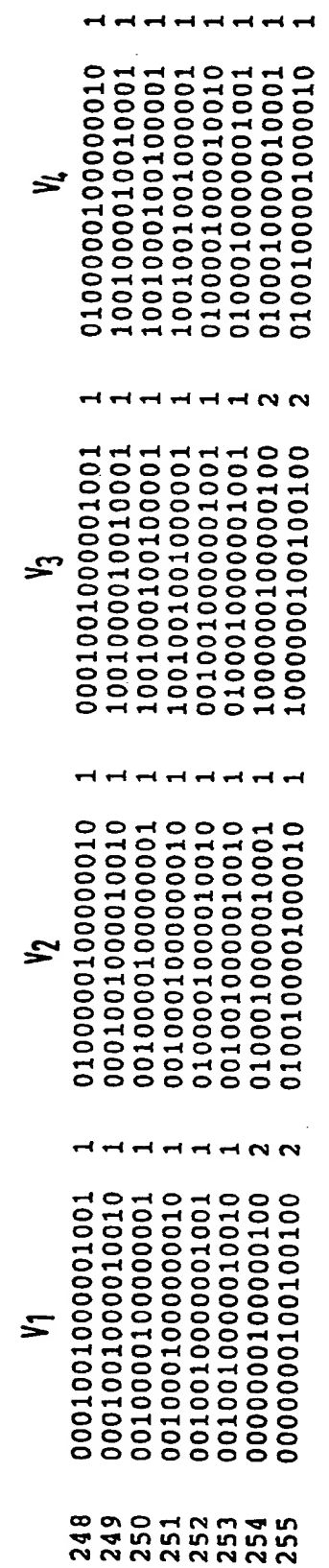
BNSDOCID: <WO 9522802A2_I_>





| | $V_1$ | | $V_2$ | | $V_3$ | | $V_4$ | |
|---|---|---|---|---|---|---|---|---|
| 217 | 0000100010000100 | 3 | 0000100010000100 | 3 | 0100100100001000 | 3 | 0100100100001000 | 3 |
| 218 | 0000100100001000 | 3 | 0100000100000100 | 3 | 0000100100001000 | 3 | 0100000100000100 | 3 |
| 219 | 0001000000100000 | 3 | 0001000000100000 | 3 | 0100010001001001 | 1 | 0100010001001001 | 1 |
| 220 | 0001000100000100 | 3 | 0001000100000100 | 3 | 0100010000001000 | 2 | 0100010000001000 | 2 |
| 221 | 0001000100100100 | 3 | 0001000100100100 | 3 | 1000100000001000 | 2 | 1000100000001000 | 2 |
| 222 | 0001001000001000 | 3 | 0100000100100100 | 3 | 0001001000001000 | 3 | 0100000100100100 | 3 |
| 223 | 0001001001000100 | 3 | 0001001001000100 | 3 | 1000010001001000 | 3 | 1000010001001000 | 3 |
| 224 | 0010001000000100 | 3 | 0010001000000100 | 3 | 1001000100001000 | 3 | 1001000100001000 | 3 |
| 225 | 0010001000100100 | 3 | 0010001000100100 | 3 | 0100100010001001 | 1 | 0100100010001001 | 1 |
| 226 | 0010001001001000 | 3 | 0100001001000100 | 3 | 0010001001001000 | 3 | 0100001001000100 | 3 |
| 227 | 0010010000001000 | 3 | 0100100100000100 | 3 | 0010010000001000 | 3 | 0100100100000100 | 3 |
| 228 | 0010010001000100 | 3 | 0010010001000100 | 3 | 1000100000001000 | 3 | 1000100000001000 | 3 |
| 229 | 0010010010001000 | 3 | 0100000000100000 | 3 | 0010010010001000 | 3 | 0100000000100000 | 3 |
| 230 | 0010000001000000 | 4 | 0010000001000000 | 4 | 1000010000001001 | 1 | 1000010000001001 | 1 |
| 231 | 0000000001000001 | 1 | 0100100000100001 | 1 | 1000000001000001 | 1 | 0100100000100001 | 1 |
| 232 | 0000000010000010 | 1 | 0100010001000100 | 2 | 1000000010000010 | 1 | 0100010001000100 | 2 |
| 233 | 0000000100001001 | 1 | 0100100010000100 | 2 | 1000000100001001 | 1 | 0100100010000100 | 2 |
| 234 | 0000000100010010 | 1 | 0100000001000000 | 4 | 1000000100010010 | 1 | 0100000001000000 | 4 |
| 235 | 0000001000010001 | 1 | 0100010000100010 | 1 | 1000001000010001 | 1 | 0100010000100010 | 1 |
| 236 | 0000001000100010 | 1 | 0100010010010001 | 1 | 1000001000100010 | 1 | 0100010010010001 | 1 |
| 237 | 0000001001001001 | 1 | 0100100010010010 | 1 | 1000001001001001 | 1 | 0100100010010010 | 1 |
| 238 | 0000010000100001 | 1 | 0000010000100001 | 1 | 1001000010001001 | 1 | 1001000010001001 | 1 |
| 239 | 0000010001000010 | 1 | 0000010001000010 | 1 | 0100100010001000 | 3 | 0100100010001000 | 3 |
| 240 | 0000010010001001 | 1 | 0100100010000100 | 3 | 0000010010001001 | 1 | 0100100010000100 | 3 |
| 241 | 0000010010010010 | 1 | 0000010010010010 | 1 | 0100100010001000 | 2 | 0100100010001000 | 2 |
| 242 | 0000100001000001 | 1 | 0000100001000001 | 1 | 1000000100000000 | 4 | 1000000100000000 | 4 |
| 243 | 0000100010000010 | 1 | 0000100010000010 | 1 | 1000010000000010 | 1 | 1000010000000010 | 1 |
| 244 | 0000100100001001 | 1 | 0100000010000001 | 1 | 0000100100001001 | 1 | 0100000010000001 | 1 |
| 245 | 0000100100010010 | 1 | 0000100100010010 | 1 | 1000100000010010 | 1 | 1000100000010010 | 1 |
| 246 | 0001000010000001 | 1 | 0001000010000001 | 1 | 1001000000010001 | 1 | 1001000000010001 | 1 |
| 247 | 0001000100000010 | 1 | 0001000100000010 | 1 | 1001000000100010 | 1 | 1001000000100010 | 1 |

FIG. 2H



| | $V_1$ | | $V_2$ | | $V_3$ | | $V_4$ | |
|---|---|---|---|---|---|---|---|---|
| 248 | 0001001000001001 | 1 | 0100000100000010 | 1 | 0001001000001001 | 1 | 0100000100000010 | 1 |
| 249 | 0001001000010010 | 1 | 0001001000010010 | 1 | 1001000010010001 | 1 | 1001000010010001 | 1 |
| 250 | 0010000100000001 | 1 | 0010000100000001 | 1 | 1001000100100001 | 1 | 1001000100100001 | 1 |
| 251 | 0010001000000010 | 1 | 0010001000000010 | 1 | 1001001001000001 | 1 | 1001001001000001 | 1 |
| 252 | 0010010000001001 | 1 | 0100001000010010 | 1 | 0010010000001001 | 1 | 0100010000010010 | 1 |
| 253 | 0010010000010010 | 1 | 0010010000010010 | 1 | 0100010000001001 | 1 | 0100010000001001 | 1 |
| 254 | 0000000100000100 | 2 | 0100010000010001 | 1 | 1000000100000100 | 2 | 0100010000010001 | 1 |
| 255 | 0000000100100100 | 2 | 0100100001000010 | 1 | 1000000100100100 | 2 | 0100100001000010 | 1 |

FIG. 2 I



BNSDOCID: <WO___9522802A2_I_>

| | $V_1$ | | $V_2$ | | $V_3$ | | $V_4$ | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0001001000000000 | 4 | 0001001000000000 | 4 | 1001000001001000 | 2 | 1001000001001000 | 2 |
| 1 | 0000100100000000 | 4 | 0000100100000000 | 4 | 1001000001001000 | 3 | 1001000001001000 | 3 |
| 2 | 0000010010000000 | 4 | 0000010010000000 | 4 | 1001000000001001 | 1 | 1001000000001001 | 1 |
| 3 | 0000001001000000 | 4 | 0100100000000010 | 1 | 1000001001000000 | 4 | 0100100000000010 | 1 |
| 4 | 0000000100100000 | 3 | 0100010000000001 | 1 | 1000000100100000 | 3 | 0100010000000001 | 1 |
| 5 | 0000000010010000 | 3 | 0100001000000000 | 4 | 1000000010010000 | 3 | 0100001000000000 | 4 |
| 6 | 0000000001001000 | 3 | 0100100100100000 | 2 | 1000000001001000 | 3 | 0100100100100000 | 2 |
| 7 | 0000000100100000 | 2 | 0100000100000000 | 4 | 1000000100100000 | 2 | 0100000100000000 | 4 |
| 8 | 0000000010010000 | 2 | 0100100010010000 | 3 | 1000000010010000 | 2 | 0100100010010000 | 3 |
| 9 | 0000000001001000 | 2 | 0100100000000100 | 2 | 1000000001001000 | 2 | 0100100000000100 | 2 |
| 10 | 0010001000000000 | 4 | 0010001000000000 | 4 | 1001001001000000 | 4 | 1001001001000000 | 4 |
| 11 | 0001000100000000 | 4 | 0001000100000000 | 4 | 0100100001001000 | 3 | 0100100001001000 | 3 |
| 12 | 0000100010000000 | 4 | 0000100010000000 | 4 | 1001000100100000 | 3 | 1001000100100000 | 3 |
| 13 | 0000010001000000 | 4 | 0000010001000000 | 4 | 1001000010010000 | 3 | 1001000010010000 | 3 |
| 14 | 0000001000100000 | 3 | 0100100000000100 | 3 | 1000001000100000 | 3 | 0100100000000100 | 3 |
| 15 | 0000000100010000 | 3 | 0100100010010000 | 2 | 1000000100010000 | 3 | 0100100010010000 | 2 |
| 16 | 0000000010001000 | 3 | 0100010000000010 | 1 | 1000000010001000 | 3 | 0100010000000010 | 1 |
| 17 | 0000000001000100 | 3 | 0100001000000001 | 1 | 1000000001000100 | 3 | 0100001000000001 | 1 |
| 18 | 0000001000100000 | 2 | 0100100000100100 | 3 | 1000001000100000 | 2 | 0100100000100100 | 3 |
| 19 | 0000000100010000 | 2 | 0100100100100000 | 3 | 1000000100010000 | 2 | 0100100100100000 | 3 |
| 20 | 0000000010001000 | 2 | 0100100000100100 | 2 | 1000000010001000 | 2 | 0100100000100100 | 2 |
| 21 | 0000000001000100 | 2 | 0100100000010010 | 1 | 1000000001000100 | 2 | 0100100000010010 | 1 |
| 22 | 0010010000000001 | 1 | 0010010000000001 | 1 | 1001000000100100 | 3 | 1001000000100100 | 3 |
| 23 | 0001001000000001 | 1 | 0001001000000001 | 1 | 1001000000000100 | 3 | 1001000000000100 | 3 |
| 24 | 0000100100000001 | 1 | 0000100100000001 | 1 | 1001000100100000 | 2 | 1001000100100000 | 2 |
| 25 | 0000010010000001 | 1 | 0000010010000001 | 1 | 1001000010010000 | 2 | 1001000010010000 | 2 |
| 26 | 0000001001000001 | 1 | 0100010000000100 | 3 | 1000001001000001 | 1 | 0100010000000100 | 3 |
| 27 | 0000000100100001 | 1 | 0100010000010010 | 1 | 1000000100100001 | 1 | 0100010000010010 | 1 |
| 28 | 0000000010010001 | 1 | 0100100100010000 | 2 | 1000000010010001 | 1 | 0100100100010000 | 2 |
| 29 | 0000000001001001 | 1 | 0100100100100001 | 1 | 1000000001001001 | 1 | 0100100100100001 | 1 |
| 30 | 0010000100000000 | 4 | 0010000100000000 | 4 | 1001000000100100 | 2 | 1001000000100100 | 2 |

FIG. 3A

BNSDOCID: <WO__9522802A2_I>

| | $V_1$ | | $V_2$ | | $V_3$ | | $V_4$ | |
|---|---|---|---|---|---|---|---|---|
| 31 | 0001000010000000 | 4 | 0001000010000000 | 4 | 1001000000000100 | 2 | 1001000000000100 | 2 |
| 32 | 0000100001000000 | 4 | 0000100001000000 | 4 | 0100100000001001 | 1 | 0100100000001001 | 1 |
| 33 | 0000010000100000 | 3 | 0000010000100000 | 3 | 1001000000010010 | 1 | 1001000000010010 | 1 |
| 34 | 0000001000010000 | 3 | 0100100010010001 | 1 | 1000001000010000 | 3 | 0100100010010001 | 1 |
| 35 | 0000000100001000 | 3 | 0100100000010001 | 1 | 1000000100001000 | 3 | 0100100000010001 | 1 |
| 36 | 0000000010000100 | 3 | 0100000010000000 | 4 | 1000000010000100 | 3 | 0100000010000000 | 4 |
| 37 | 0000010000100000 | 2 | 0000010000100000 | 2 | 1000100000000010 | 1 | 1000100000000010 | 1 |
| 38 | 0000001000010000 | 2 | 0100010000100100 | 3 | 1000001000010000 | 2 | 0100010000100100 | 3 |
| 39 | 0000000100001000 | 2 | 0100010010010000 | 2 | 1000000100001000 | 2 | 0100010010010000 | 2 |
| 40 | 0000000010000100 | 2 | 0100001000000010 | 1 | 1000000010000100 | 2 | 0100001000000010 | 1 |
| 41 | 0010010000000010 | 1 | 0010010000000010 | 1 | 1000010000000001 | 1 | 1000010000000001 | 1 |
| 42 | 0010001000000001 | 1 | 0010001000000001 | 1 | 1000001000000000 | 4 | 1000001000000000 | 4 |
| 43 | 0001001000000010 | 1 | 0001001000000010 | 1 | 0100100001001000 | 2 | 0100100001001000 | 2 |
| 44 | 0001000100000001 | 1 | 0001000100000001 | 1 | 1001000001001001 | 1 | 1001000001001001 | 1 |
| 45 | 0000100100000010 | 1 | 0000100100000010 | 1 | 1001000010001000 | 3 | 1001000010001000 | 3 |
| 46 | 0000100010000001 | 1 | 0000100010000001 | 1 | 1001000000001000 | 3 | 1001000000001000 | 3 |
| 47 | 0000010010000010 | 1 | 0000010010000010 | 1 | 1000100000001001 | 1 | 1000100000001001 | 1 |
| 48 | 0000010001000001 | 1 | 0000010001000001 | 1 | 1000100001001000 | 3 | 1000100001001000 | 3 |
| 49 | 0000001001000010 | 1 | 0100000100000001 | 1 | 1000001001000010 | 1 | 0100000100000001 | 1 |
| 50 | 0000001000100001 | 1 | 0100100001000100 | 3 | 1000001000100001 | 1 | 0100100001000100 | 3 |
| 51 | 0000000100100010 | 1 | 0100010010010000 | 3 | 1000000100100010 | 1 | 0100010010010000 | 3 |
| 52 | 0000000100010001 | 1 | 0100010000100100 | 2 | 1000000100010001 | 1 | 0100010000100100 | 2 |
| 53 | 0000000010010010 | 1 | 0100010000000100 | 2 | 1000000010010010 | 1 | 0100010000000100 | 2 |
| 54 | 0000000010001001 | 1 | 0100100000100010 | 1 | 1000000010001001 | 1 | 0100100000100010 | 1 |
| 55 | 0000000001000010 | 1 | 0100100100010000 | 3 | 1000000001000010 | 1 | 0100100100010000 | 3 |
| 56 | 0010000010000000 | 4 | 0010000010000000 | 4 | 0100100000001000 | 3 | 0100100000001000 | 3 |
| 57 | 0001000001000000 | 4 | 0001000001000000 | 4 | 1001000010001000 | 2 | 1001000010001000 | 2 |
| 58 | 0010010010010000 | 3 | 0010010010010000 | 3 | 1001000000001000 | 2 | 1001000000001000 | 2 |
| 59 | 0010010001001000 | 3 | 0100100001000100 | 2 | 0010010001001000 | 3 | 0100100001000100 | 2 |
| 60 | 0010010000100100 | 3 | 0010010000100100 | 3 | 0100100000001000 | 2 | 0100100000001000 | 2 |
| 61 | 0010010000000100 | 3 | 0010010000000100 | 3 | 0100010001001000 | 2 | 0100010001001000 | 2 |

FIG. 3B

BNSDOCID: <WO__9522802A2_1_>

BNSDOCID: <WO__9522802A2_I_>

| | $V_1$ | | $V_2$ | | $V_3$ | | $V_4$ | |
|---|---|---|---|---|---|---|---|---|
| 62 | 0001001001001000 | 3 | 0100100100010001 | 1 | 0001001001001000 | 3 | 0100100100010001 | 1 |
| 63 | 0001001000100100 | 3 | 0001001000100100 | 3 | 0100010001001000 | 3 | 0100010001001000 | 3 |
| 64 | 0001001000000100 | 3 | 0001001000000100 | 3 | 1001001000100000 | 3 | 1001001000100000 | 3 |
| 65 | 0000100100100100 | 3 | 0000100100100100 | 3 | 1001000100010000 | 3 | 1001000100010000 | 3 |
| 66 | 0000100100000100 | 3 | 0000100100000100 | 3 | 1001000001000100 | 3 | 1001000001000100 | 3 |
| 67 | 0000100000100000 | 3 | 0000100000100000 | 3 | 1000100100100000 | 3 | 1000100100100000 | 3 |
| 68 | 0000010010000100 | 3 | 0000010010000100 | 3 | 1000100010010000 | 3 | 1000100010010000 | 3 |
| 69 | 0000010000010000 | 3 | 0000010000010000 | 3 | 1000100000100100 | 3 | 1000100000100100 | 3 |
| 70 | 0000001001000100 | 3 | 0100100000010000 | 2 | 1000001001000100 | 3 | 0100100000010000 | 2 |
| 71 | 0000001000001000 | 3 | 0100100000010000 | 3 | 1000001000001000 | 3 | 0100100000010000 | 3 |
| 72 | 0000000100100100 | 3 | 0100010001000100 | 3 | 1000000100100100 | 3 | 0100010001000100 | 3 |
| 73 | 0000000100000100 | 3 | 0100001000100100 | 3 | 1000000100000100 | 3 | 0100001000100100 | 3 |
| 74 | 0010010010010000 | 2 | 0010010010010000 | 2 | 1000100000000100 | 3 | 1000100000000100 | 3 |
| 75 | 0010010001001000 | 2 | 0100001000000100 | 3 | 0010010001001000 | 2 | 0100001000000100 | 3 |
| 76 | 0010010000100100 | 2 | 0010010000100100 | 2 | 1000100001001000 | 2 | 1000100001001000 | 2 |
| 77 | 0010010000000100 | 2 | 0010010000000100 | 2 | 1001001000100000 | 2 | 1001001000100000 | 2 |
| 78 | 0001001001001000 | 2 | 0100100100100010 | 1 | 0001001001001000 | 2 | 0100100100100010 | 1 |
| 79 | 0001001000100100 | 2 | 0001001000100100 | 2 | 1001000100010000 | 2 | 1001000100010000 | 2 |
| 80 | 0001001000000100 | 2 | 0001001000000100 | 2 | 1001000001000100 | 2 | 1001000001000100 | 2 |
| 81 | 0000100100100100 | 2 | 0000100100100100 | 2 | 1000100100100000 | 2 | 1000100100100000 | 2 |
| 82 | 0000100100000100 | 2 | 0000100100000100 | 2 | 1000100010010000 | 2 | 1000100010010000 | 2 |
| 83 | 0000100000100000 | 2 | 0000100000100000 | 2 | 1000100000100100 | 2 | 1000100000100100 | 2 |
| 84 | 0000010010000100 | 2 | 0000010010000100 | 2 | 1000100000000100 | 2 | 1000100000000100 | 2 |
| 85 | 0000010000010000 | 2 | 0000010000010000 | 2 | 0100100001001001 | 1 | 0100100001001001 | 1 |
| 86 | 0000001001000100 | 2 | 0100001000100100 | 2 | 1000001001000100 | 2 | 0100001000100100 | 2 |
| 87 | 0000001000001000 | 2 | 0100001000000100 | 2 | 1000001000001000 | 2 | 0100001000000100 | 2 |

FIG. 3c

| IW | SW | LB | D S V | C W | CS | dDSV | DSVN | L B N | SWN |
|---|---|---|---|---|---|---|---|---|---|
| "2" | S1 | H | 0 | 0 0 1 0 0 0 0 0 0 1 0 0 1 0 0 | * | − 6 | − 6 | 1 | S2 |
| | | | | 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0 | | + 10 | + 10 | 0 | S4 |
| "8" | S2 | L | − 6 | 0 0 1 0 0 0 0 0 1 0 0 1 0 0 0 | * | − 6 | − 0 | 1 | S3 |
| | | | | 0 1 0 0 1 0 0 0 1 0 0 1 0 0 0 | | + 12 | − 18 | 0 | S3 |
| "100" | S3 | H | 0 | 1 0 0 0 0 1 0 0 0 0 0 1 0 0 0 | 1 * | − 2 | − 2 | 0 | S1 |
| "230" | S1 | H | − 2 | 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 | * | + 2 | 0 | 0 | S4 |
| "0" | S4 | H | 0 | 0 1 0 0 0 0 0 0 0 1 0 0 1 0 0 | | − 8 | − 8 | 1 | S2 |
| | | | | 1 0 0 1 0 0 0 0 0 1 0 0 1 0 0 | * | + 4 | + 4 | 0 | S2 |
| "61" | S2 | H | + 4 | 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 | 1 * | − 2 | + 2 | 0 | S1 |
| | | | | 0 0 1 0 0 1 0 0 0 0 0 0 0 1 0 | 0 | + 3 | + 7 | 1 | S2 |
| "255" | S1 | H | + 2 | 0 0 0 0 0 0 0 1 0 0 1 0 0 1 0 | 0 * | + 4 | + 6 | 1 | S1 |

FIG. 4



BNSDOCID: <WO__9522802A2_I_>

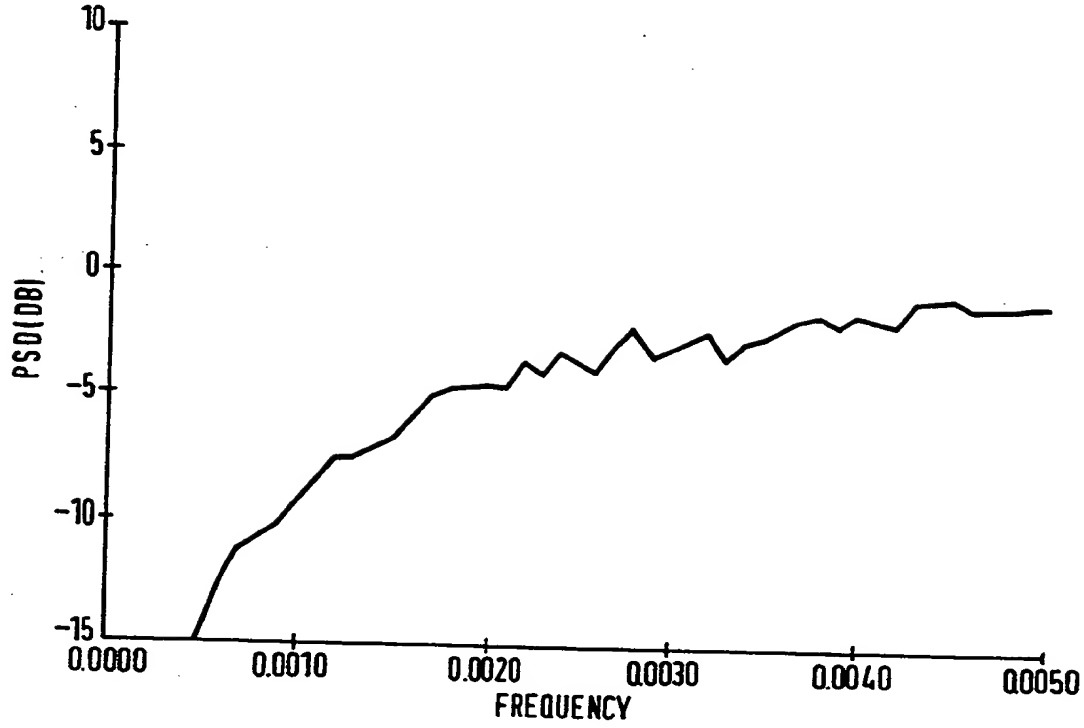



FIG. 5a

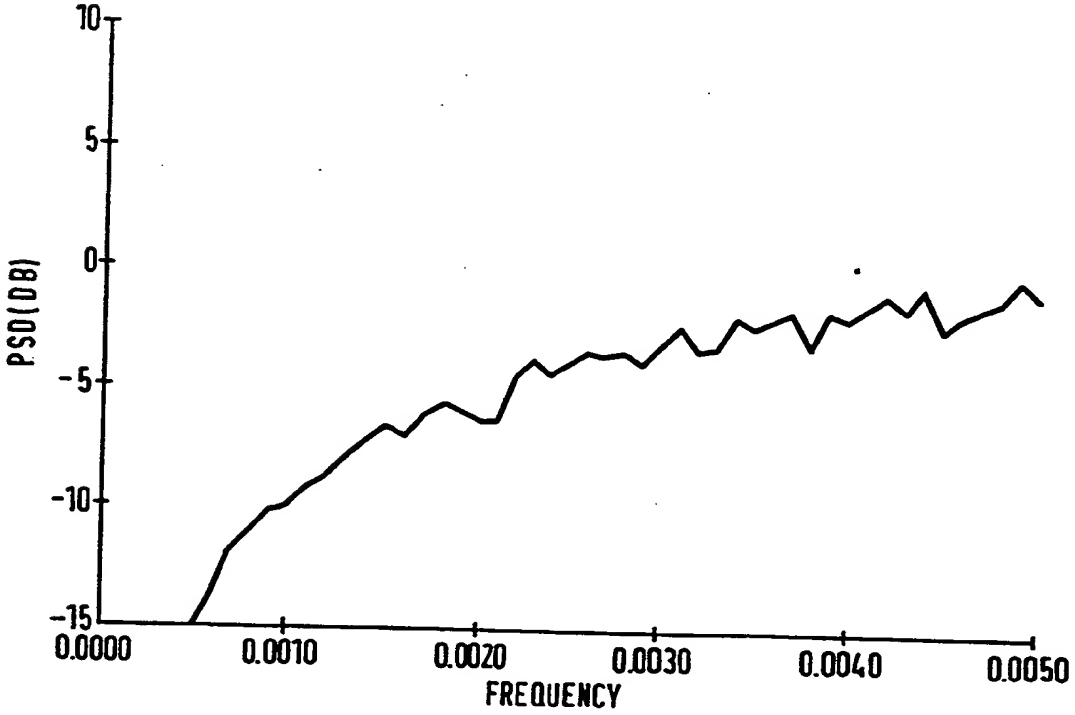



FIG. 5b

BNSDOCID: <WO___9522802A2_I_>

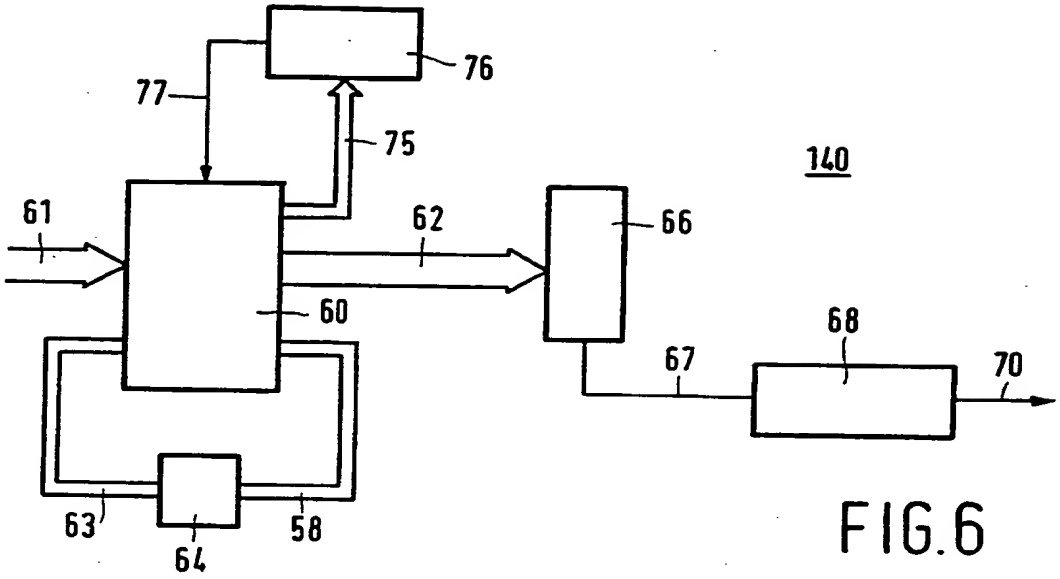



FIG.6

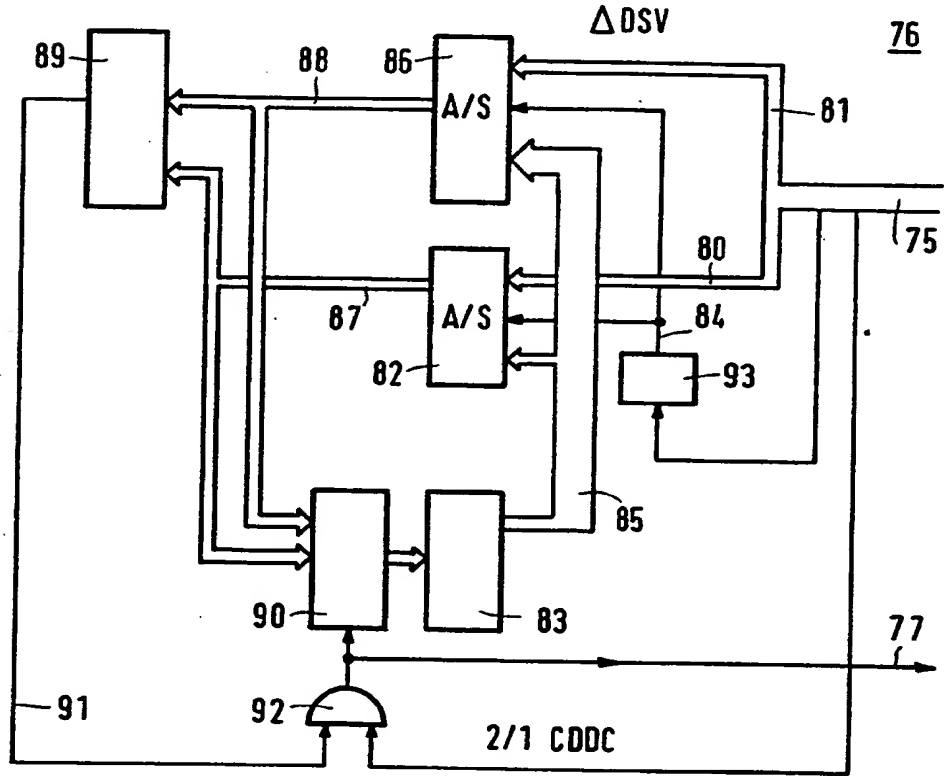



FIG.7

BNSDOCID: <WO___9522802A2_I_>

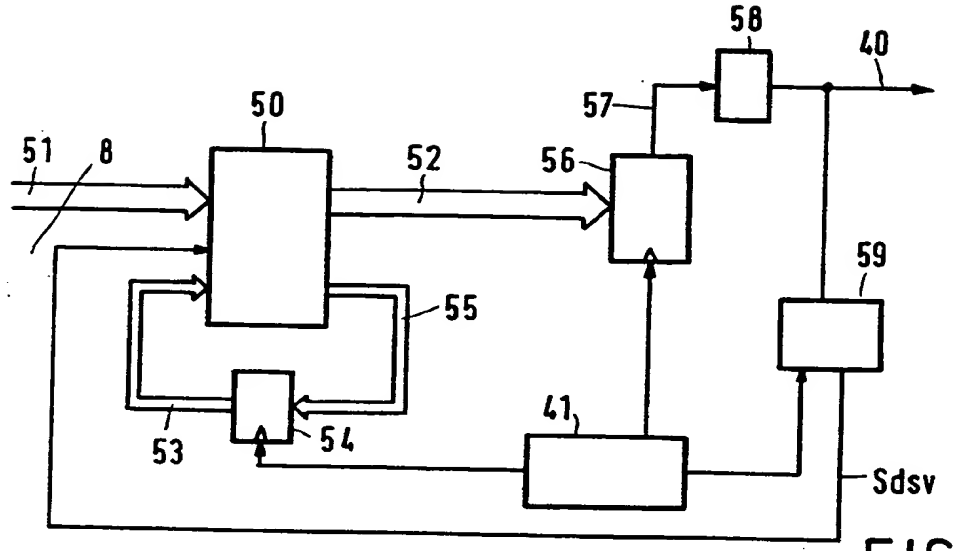



FIG.8

X1 . . . . . X13 . . . . . X26

1 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 ~100

0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 ~101

FIG.9

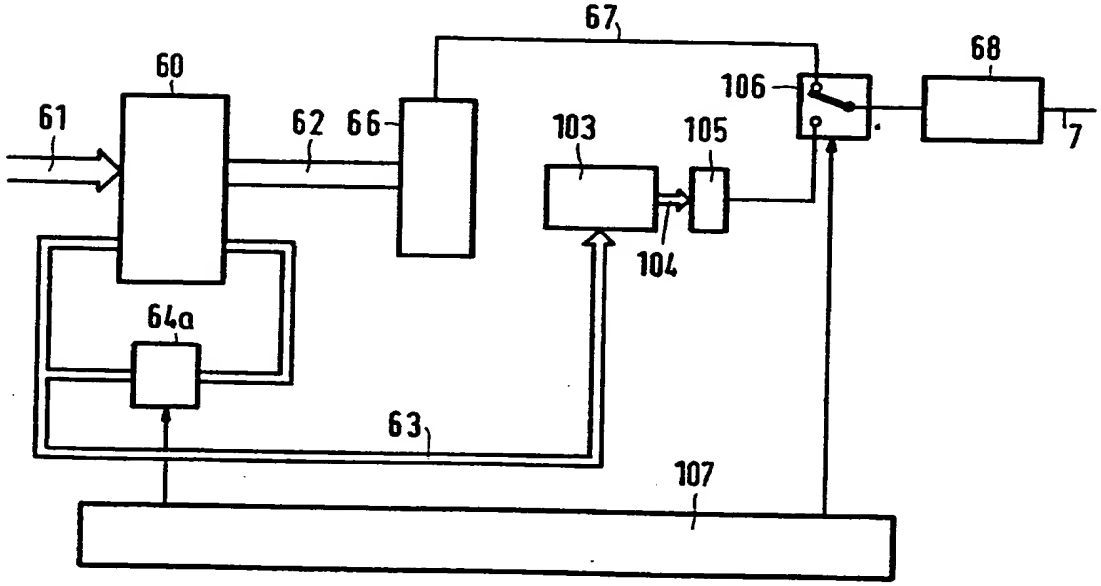



FIG.10

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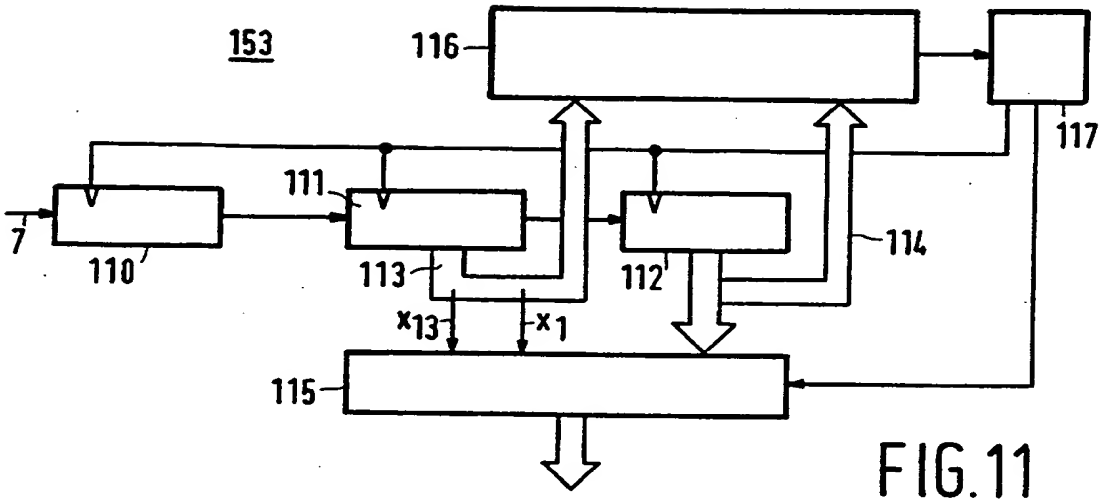


FIG.11

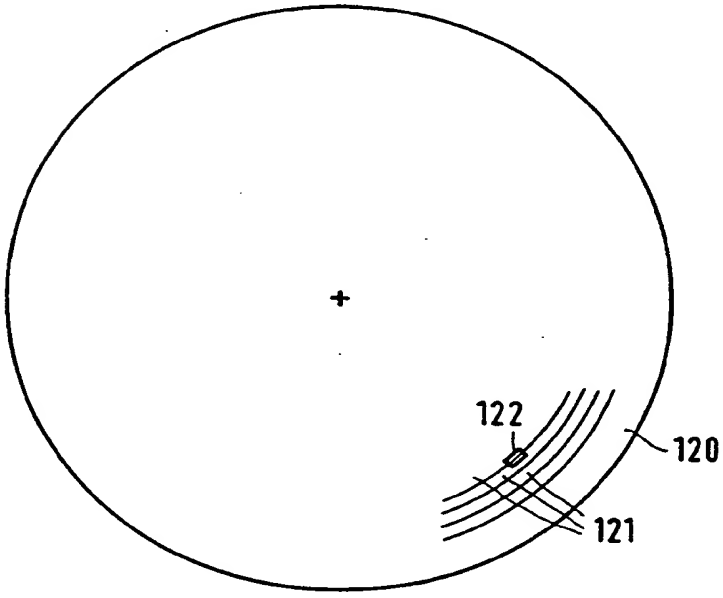


FIG.12

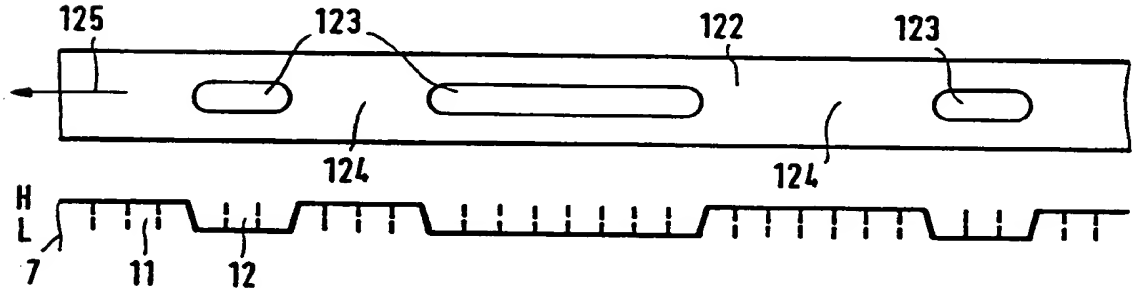


FIG.13

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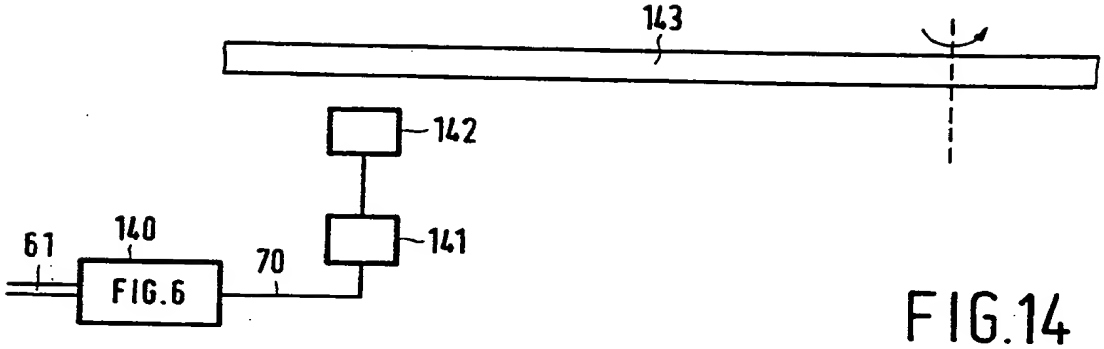


FIG.14

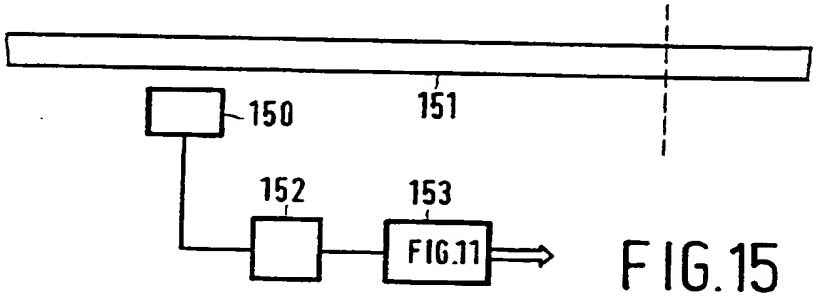


FIG.15

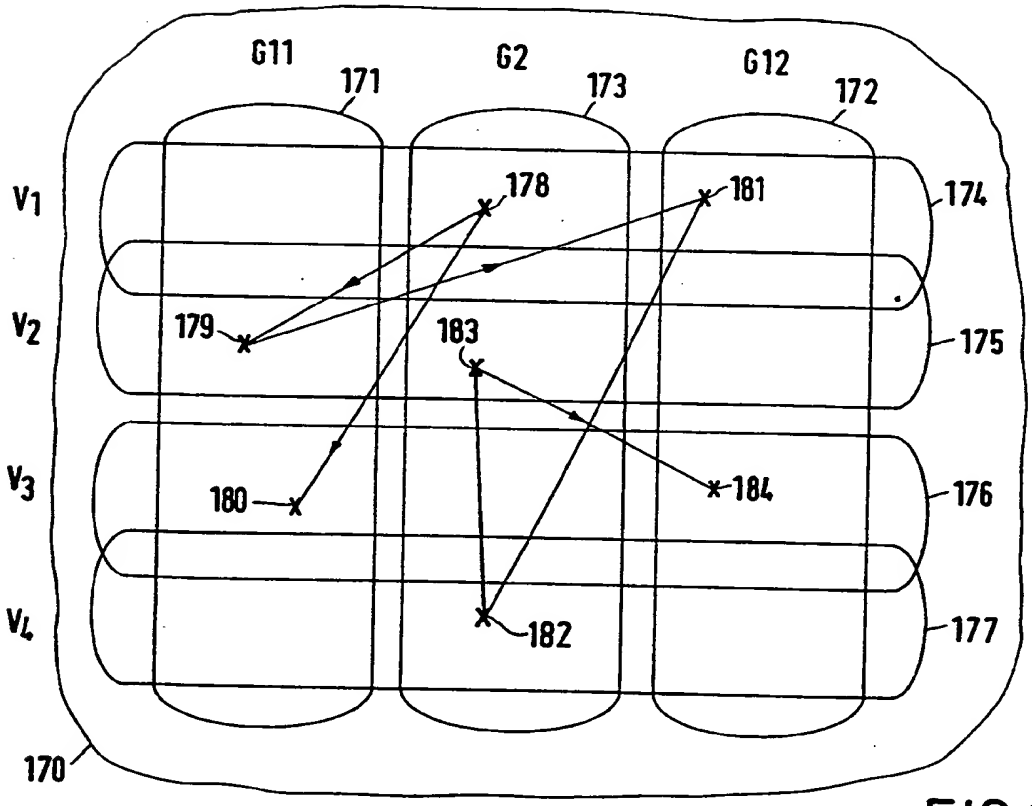


FIG.17

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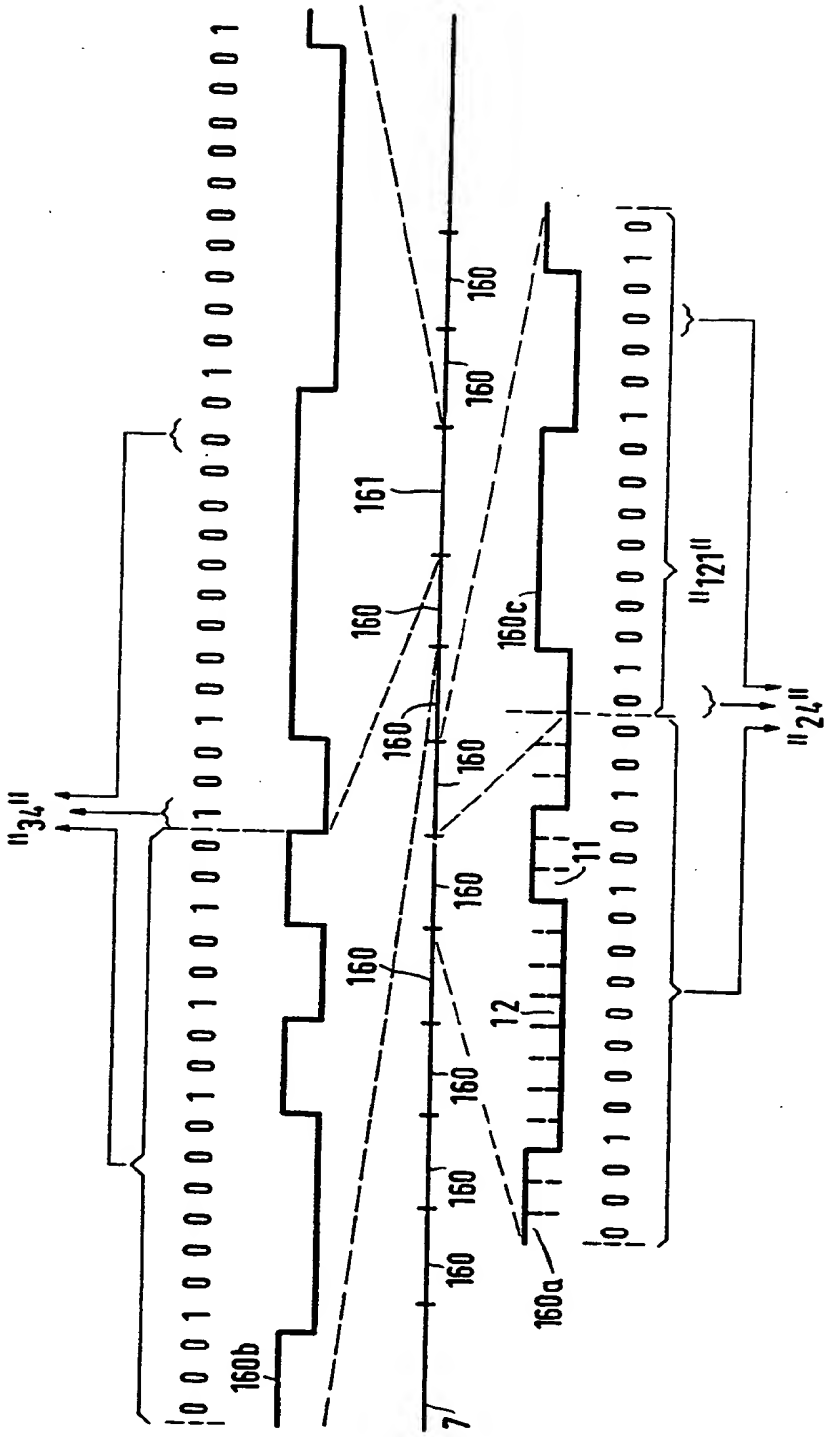


FIG.16

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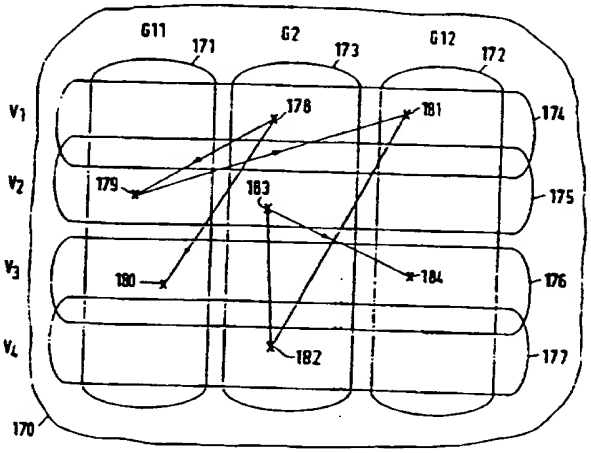
(54) Title: METHOD OF CONVERTING A SERIES OF M-BIT INFORMATION WORDS TO A MODULATED SIGNAL, METHOD OF PRODUCING A RECORD CARRIER, CODING DEVICE, DECODING DEVICE, RECORDING DEVICE, READING DEVICE, SIGNAL, AS WELL AS A RECORD CARRIER




(57) Abstract

The Patent Applications relates to a method of converting a series of m-bit information words (1) to a modulated signal (7). For each information word from the series an n-bit code word (4) is delivered. The delivered code words (4) are converted to the modulated signal (7). The code words (4) are distributed over at least one group (G11, G12) of a first type and at least one group (G2) of a second type. For the delivery of each of the code words belonging to the group (G11, G12) of the first type the associated group establishes a coding state (S1, S4) of the first type. When each of the code words (4) belonging to the group (G2) of the second type is delivered, a coding state (S2, S3) of the second type is established which is determined by an information word belonging to the delivered code word. When one of the code words (4) is assigned to the received information word (1), this code word is selected from a set (V1, V2, V3, V4) of code words which depends on the coding states (S1, S2, S3, S4). The sets of code words (V2, V3) belonging to the coding states (S1, S2) of the second type are disjunct. In this coding method the number of unique bit combinations that may be established by the code words in the series are enlarged. The modulated signal (7) thus obtained may be reconverted to information words (4) by first converting the modulated signal (7) to a series of code words (4) and then assigning an information word (1) to each of the code words from the series in dependence on the code word to be converted and also in dependence on the logical values of the bit string bits which are situated at predetermined positions relative to the code word. Furthermore, a recording device and a reading device are disclosed.

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# INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER

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According to International Patent Classification (IPC) or to both national classification and IPC

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

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| A | EP 0193153 A3 (MATSUSHITA ELECTRIC INDUSTRIAL CO, LTD), 3 Sept 1986 (03.09.86), see whole document | 1-38 |
| A | DE 3215179 A1 (SONY CORP.), 9 December 1982 (09.12.82), see whole document | 1-38 |

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| 4 Sept 1995 | 05 -09- 1995 |
| Name and mailing address of the ISA/<br>Swedish Patent Office<br>Box 5055, S-102 42 STOCKHOLM<br>Facsimile No. +46 8 666 02 86 | Authorized officer<br>Jan Kossmann<br>Telephone No. +46 8 782 25 00 |

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31/07/95

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